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A TELETYPEWRITER ADAPTER UNIT FOR THE DRISROTE APERTURED PLATE MEMORY

TECHNICAL DOCUMENTARY REPORT ASD-TDR-62-1058

MARCH 15, 1963

ELECTROMAGNETIC WARFARE COMMUNICATION LABORATORY
AERONAUTICAL SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO

PROJECT NO. 4335, TASK NO. 433517
PREPARED UNDER CONTRACT NO. AF 33(657)-7905
BY:

AEROSPACE COMMUNICATIONS AND CONTROLS DIVISION
DEFENSE ELECTRONIC PRODUCTS
RADIO CORPORATION OF AMERICA
CAMDEN, NEW JERSEY

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9B

FOREWORD

This report was prepared by the Radio Corporation of America, Camden, New Jersey, on Air Force Contract AF 33(657)-7905 under Task No. 433517 of Project No. 4335, "A Teletypewriter Adapter Unit for the DRISROTE Apertured Plate Memory." The work was administered under the direction of the Electronic Warfare and Communications Laboratory, Aeronautical Systems Division. Mr. Robert Matson was project engineer for the Laboratory.

The studies presented began in May 1962 and were concluded in December 1962. They represent a joint effort of the Aerospace Communications and Controls Division of the Radio Corporation of America in which Mr. E. J. Mozzi was the project leader responsible for the task.

The chief contributors were Mr. W. A. McNamara and Mr. W. V. Dix both of whom are design and development engineers.

This report is the final report and concludes the work on contract AF 33(657)-7905. The contractors report number is CR-63-591-2.

This report is unclassified.

ABSTRACT

This research was initiated to demonstrate the use of the DRISROTE equipment ~~AF 33(616)6280~~ as a storage device for teletypewriter information. The particular teletypewriter used is a Kleinschmidt Model 120 which utilizes serial 7.42 unit Baudot Code. The DRISROTE equipment is an apertured plate memory capable of storing 15,360 bits of information with input and output rates up to one megacycle. To achieve the objective, an adapter was designed and constructed, and modifications were made to the teletypewriter and DRISROTE. Teletypewriter-generated messages were stored in DRISROTE, reconstituted, read out of DRISROTE, and printed by the teletypewriter with good fidelity.

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SECTION I

INTRODUCTION

A. PURPOSE OF REPORT

This Technical Report is a final report to ASD on the work performed and the equipment designed under Contract AF 33(657)-7905. The report is submitted in accordance with the requirements of Item I of the contract.

B. SCOPE OF REPORT

This report describes the complete effort on the program during the logic revision and circuit changes performed on the equipment. The experimental system for demonstration, including the required modifications to the teletypewriter and DRISROTE equipment, is described in detail. Instructions for operation and sufficient data for maintenance of the revisions are included in an appendix.

C. PROGRAM OBJECTIVE

This contract was specifically awarded to implement the demonstration of the operational characteristics of the DRISROTE system with a teletypewriter. It was desired that a minimum of modification be performed on the teletypewriter and DRISROTE equipment. The number of controls required after initial turn-on were to be kept to a minimum and standard DRISROTE circuit boards were to be used whenever possible. The system which was implemented complies with the listed objectives.

Manuscript released by the author 1 March 1963 for publication as an ASD Technical Documentary Report.

D. SUMMARY

As a result of the short time cycle of the contract, the program was organized into several parallel efforts.

1. Test and repair of Government Furnished Equipment (GFE).

2. Detailed examination of the requirements for the design of the adapter logic.

3. Modification of the GFE to accomplish the task, and fabrication of parts for the adapter.

4. Assembly and test of the system and report writing.

Tasks 1 and 2 were conducted concurrently, followed by Task 3; Task 4 was started before Task 3 was completed. Task 1 became a major stumbling block because of many hours of operation on the DRISROTE. This system was to utilize a type 105 Teleprinter which was designed to provide and accept parallel signals. Since this machine was not available, the system was designed to operate with a Kleinschmidt Model 120 Teletypewriter. The latter operates with serial 7.42 Baudot code and therefore required several major changes in the design concept of the adapter. In addition, a separate timing generator which runs at the teletype rate was needed, and information had to be processed and stored on a bit-by-bit basis rather than one character at a time.

SECTION II

SYSTEM DESCRIPTION

A. DRISROTE CHARACTERISTICS

A complete description of the DRISROTE system can be found in WADD Technical Report #60-915.

B. TELETYPEWRITER

A complete description of the teletypewriter may be found in Department of the Army Technical Manual TM11-2225.

C. WRITE, OR TRANSMIT MODE

Signals representing one character which originate in the teletypewriter are of a non-return-to-zero (NRZ) nature and start with a space pulse. When the adapter and DRISROTE are in the "Write" mode, signal flow is as shown in Figure 1. The space pulse triggers the timing generator to supply sufficient pulses to the sampler for processing one character.

The sampler provides the dual function of sampling the teletypewriter output and creating a corresponding polarized return to zero (PRZ) message. This message is then routed to DRISROTE for storage. The process continues as keys of the teletypewriter are depressed, until the DRISROTE memory storage has been filled. At this time, DRISROTE and the control circuitry generate a signal to inhibit additional message processing. This is done by disabling the timing generator trigger input and the sampler.

D. READ, OR RECEIVE MODE

Signal flow during this mode is shown in Figure 2. Upon receipt of a manually-generated start signal, the timing generator produces a synchronization or

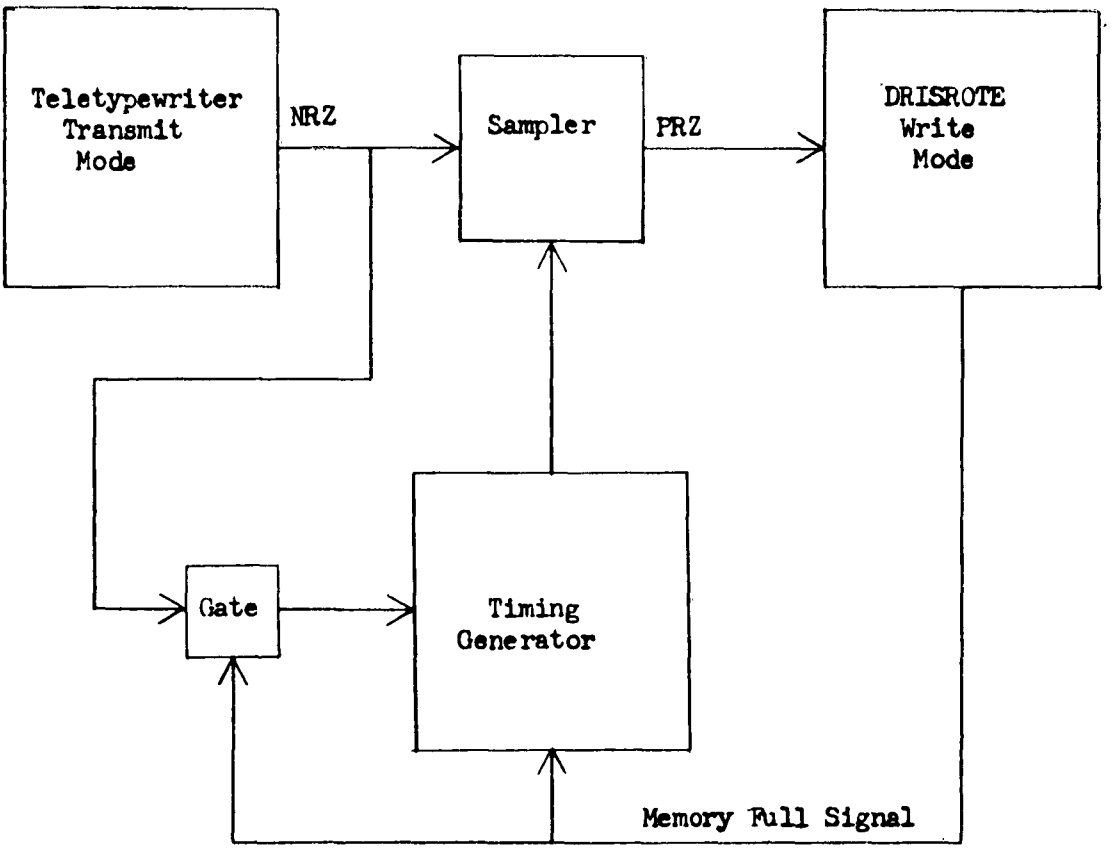


Figure 1. Input System-Block Diagram

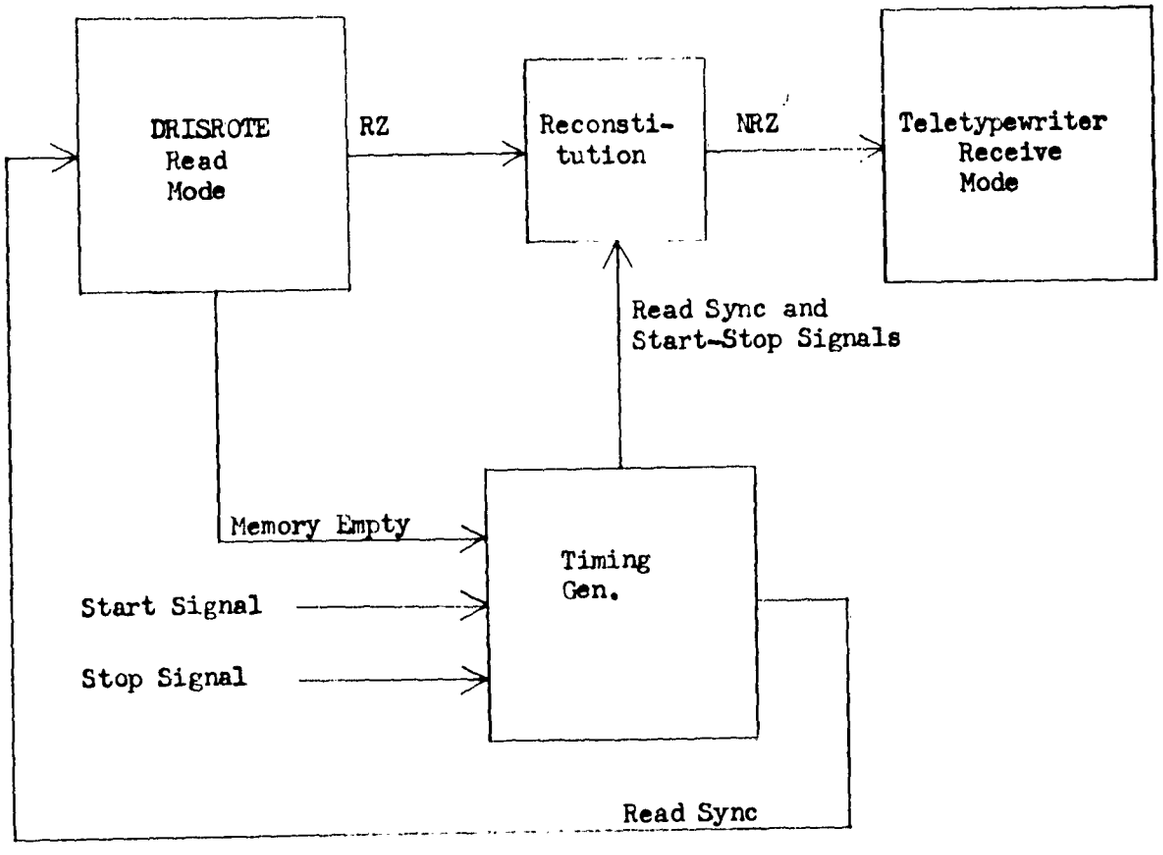


Figure 2. Output System-Block Diagram

interrogation pulse train to extract the data stored in the DRISROTE on a bit-by-bit demand basis. Simultaneously, another set of pulses is provided to the reconstitution section. One generates a non-return-to-zero signal from the DRISROTE output and the other inserts the start and stop portions of the signal required by the teletypewriter. The reconstituted signal is then converted to printed copy by the teletypewriter. When the DRISROTE memory is empty it generates a signal to stop the timing generator.

If a message of less than the full memory capacity has been stored and it is desired to stop the printing function after printout of the short message, the stop signal is generated manually by depressing the stop button on the control panel. If this is not done, the printer will continue spacing until the last memory location has been interrogated.

SECTION III

DESCRIPTION OF THE MODEL

The Adapter is briefly described here to summarize its features. A complete discussion on the theory of operation and electrical configuration of the adapter and its major components is contained in Section IV.

A. TIMING PULSE GENERATOR

A major component of the adapter is the timing pulse generator. Upon receipt of appropriate control signals, this generator provides a set of pulses one group of which is at double the normal teletypewriter bit rate. During the "Read" mode only the even numbered pulses are utilized for re-creation of the teletypewriter code, while during the "Write" mode only the odd numbered pulses are employed for processing the incoming signal. In addition, the generated pulses are utilized to drive a four-stage binary counter whose state is examined by logic gates to provide reset functions and/or suppression of certain pulses. During the write sequence, the timing generator is triggered by the first transition of the incoming signal, and provides the necessary sampling pulses for the sampler to extract the pertinent data from the incoming message. During the read mode, pulses are supplied by the timing generator to DRISROTE for data extraction and the reconstitution section, in order to recreate the original message from the stored data and insert the start and stop information.

B. RESET AND WARNING INDICATORS

To provide some of the required automatic reset features and the desired warning indicators, two additional signals were routed from DRISROTE to the adapter unit. The necessary information transfers, register reset, and flip-flop reset are automatically produced when the Read-Write switch is moved to either the "Read" or "Write" position. Control system signals via logic gates are utilized to activate lamps for "Memory Full", "Memory Empty", and "Memory Near Full" indications.

C. SIGNAL SHAPING

Due to electronic noise produced by the teletypewriter contact bounce, the contact filters were retained and signal shaping was performed in the adapter to obtain the rise and fall times required by the processing circuitry. To establish and terminate current in the teletypewriter "Mark" coil inductance with the proper timing, it was necessary to route the teletypewriter power supply voltage to the adapter for use in its output circuit.

D. WORD GENERATOR

All of the circuitry and controls required by the adapter were added to the existing word generator. This made a minimum over-all size possible and provided easy access to the word generator control logic and signal processing circuitry. A considerable portion of the word generator was utilized and augmented to implement the adapter, such as most of the control logic, the polarized return-to-zero converters, and the reset circuitry.

E. OPERATION

Operation of the unit in the original manner is still possible by means of switch S-5 in the "Normal" position. To provide teletypewriter operation, switch S-5 is placed in the "Teletype" position. Operation in the teletype mode at several standard rates is facilitated by a speed switch appropriately marked 60, 100, 1500 WPM.

F. POWER SUPPLIES

A set of adjustable voltage, current-limited supplies furnish the required voltages to operate DRISROTE, the adapter, and the control section. Six of these have a range of 0 to 20 volts, current-limited at 2 amperes and furnish ±6, ±12, and ±20 volts. The two other supplies have a range of 0 to 32 volts, current-limited at 1.5 ampere and supply ±28 volts. An additional -1.5 volts is generated in the control unit by the forward drop of two diodes which are energized via a resistor from the -6 volt supply for use as a bias in DRISROTE. The adapter, power control panel and power supplies are mounted in a desk-size relay rack, with the power supplies located near the bottom and the controls at the top for convenient access.

SECTION IV

DETAILED DESCRIPTION OF MAJOR SYSTEM COMPONENTS

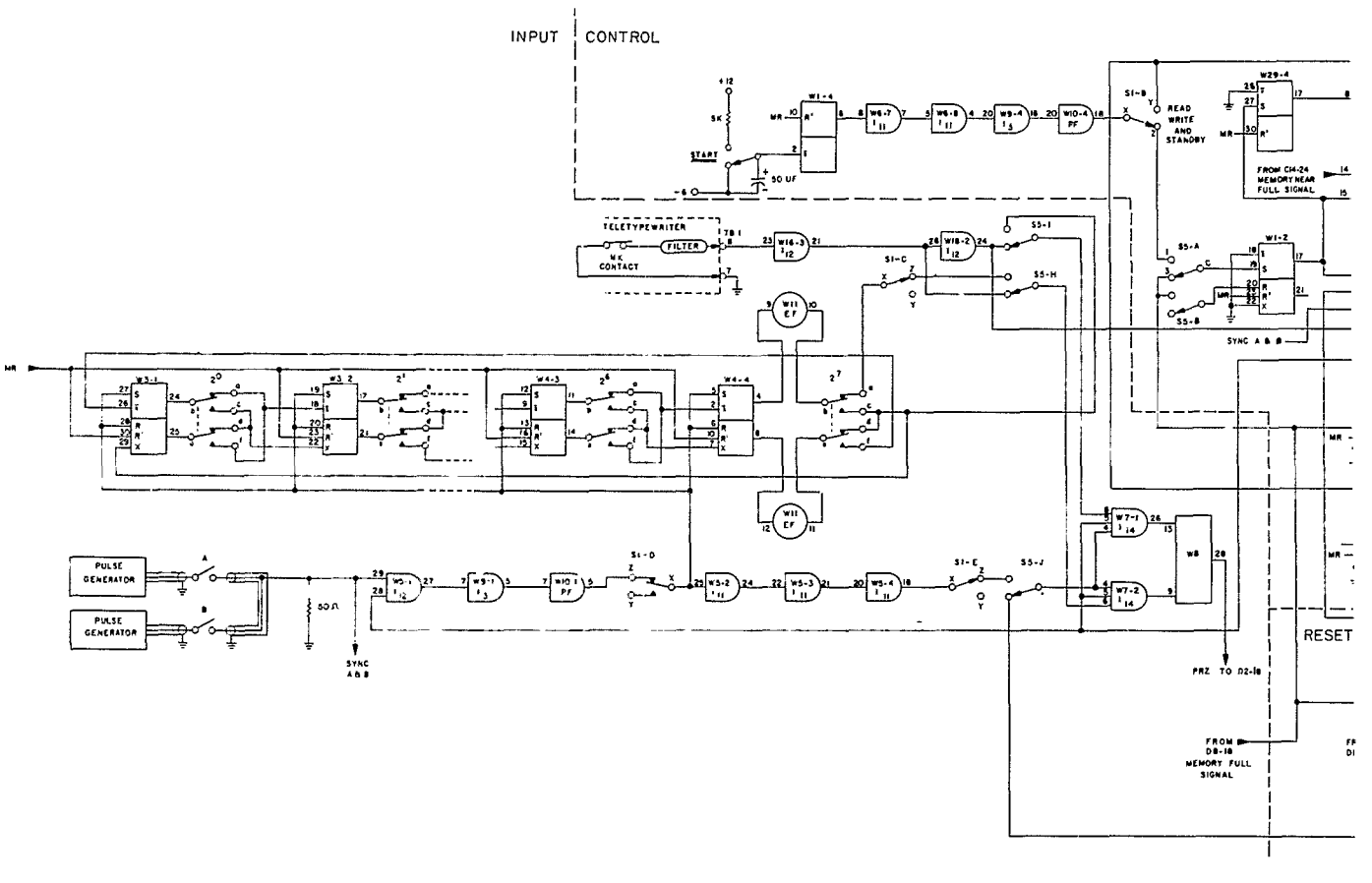
A. INPUT SAMPLER

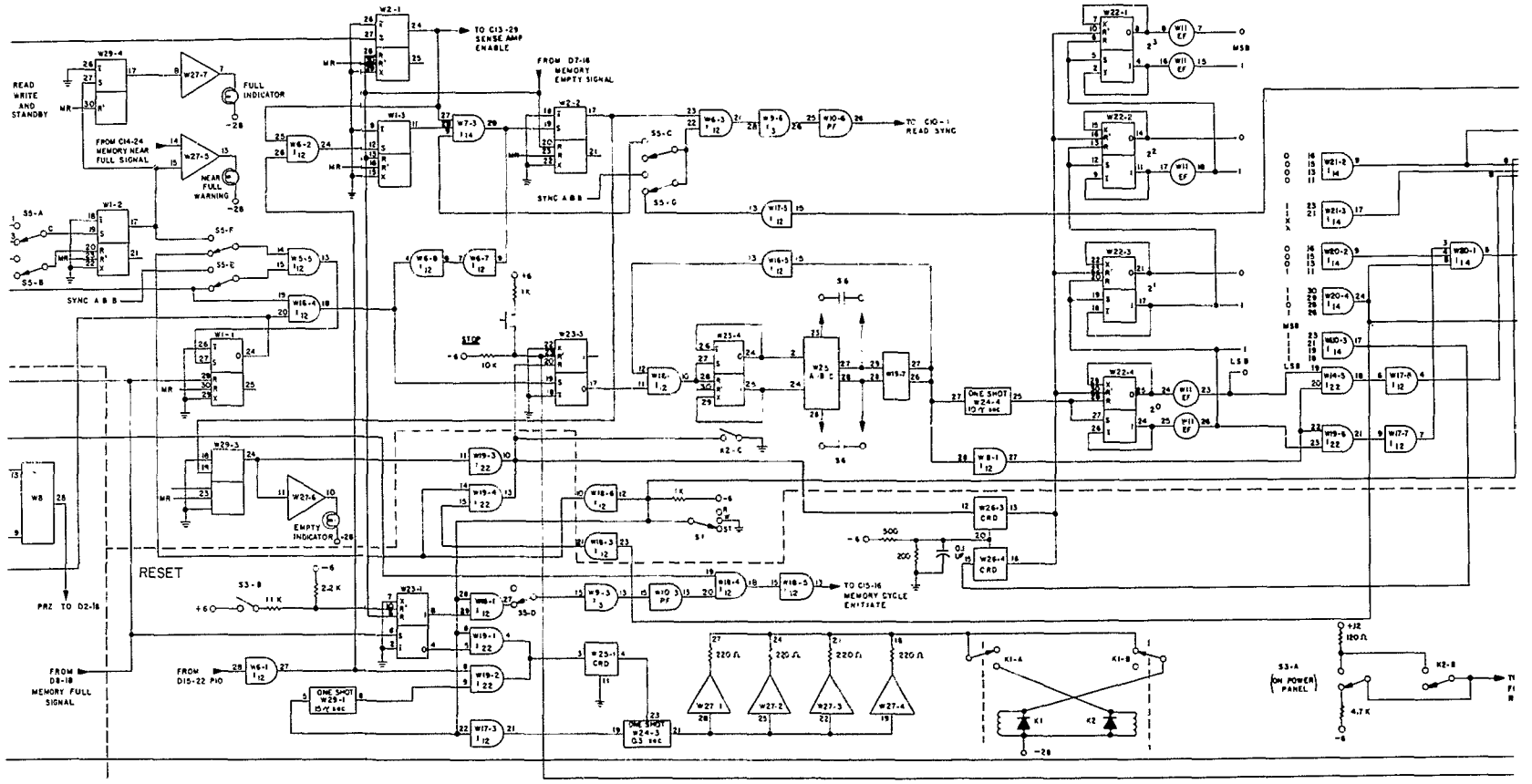
The signal supplied to DRISROTE must be in a polarized return-to-zero form. A logical "1" is represented by a positive 6-volt pulse 0.25-microsecond in length and a logical "0" by a negative 6-volt pulse of the same length. Storage is provided for 15,360 bits of information at any input rate up to one megacycle.

The teletypewriter may be manually operated by the keyboard or automatically by pre-punched tape. The signal generated by the teletypewriter is the same in either case. The standard 7.42-bit Baudot code is used to represent the characters on the keyboard. The coding for each character begins with a one-bit "space" pulse and terminates with a "mark" pulse which is at least 1.42 bits long. A "mark" corresponds to a closure of the teletypewriter MK contact shown in Figure 3. A space is represented when this switch is open. The first "space" pulse and last "mark" pulse are referred to as the "start" and "stop" pulses respectively. A unique combination of "marks" and "spaces" occurring in the five-pulse interval between the "start" and "stop" pulses identifies the character being transmitted. The total sequence of pulses is presented in serial form.

To detect this information and convert it to a form acceptable to the memory, it is necessary to strip off the "start" and "stop" pulses. The remaining information pulses must then be converted to the polarized return-to-zero form required by DRISROTE. To minimize the possibility of errors due to contact bounce and teletypewriter drift, the information pulses are passed through a filter, and then sampled near the center of each pulse. The circuitry required to perform the sampling is described in paragraph C Timing Generator.

The filtered information from the teletypewriter (Figure 3) is inverted and shaped by gates W-16-3 and W-18-2. This operation improves the rise and fall times of the "start" pulse, so that more positive triggering of the control circuitry is obtained.


INPUT
CONTROL
+12
5K
START
50 UF
-6
MR
W1-4
W6-7
W6-8
W9-4
W10-4
PF
S1-B
READ WRITE AND STANDBY
W29-4
FROM CI4-24 MEMORY NEAR FULL SIGNAL
TELETYPEWRITER
FILTER
W.K. CONTACT
W16-3
W18-2
S1-C
S5-I
S5-H
S5-A
S5-B
W1-2
SYNC A & B
W11 EF
W3-1
W3-2
W4-3
W4-4
PULSE GENERATOR
A
B
50Ω
SYNC A & B
W5-1
W9-1
W10-1
S1-D
W5-2
W5-3
W5-4
S1-E
S5-J
W7-1
W7-2
W8
PRZ TO D2-18
FROM D8-18 MEMORY FULL SIGNAL
RESET


READ WRITE AND STANDBY
FULL INDICATOR
FROM CI4-24 MEMORY NEAR FULL SIGNAL
NEAR FULL WARNING
SYNC A B B
TO C13-29 SENSE AMP ENABLE
FROM D7-16 MEMORY EMPTY SIGNAL
TO C10-1 READ SYNC
STOP
RESET
EMPTY INDICATOR
PRZ TO D2-16
FROM D8-18 MEMORY FULL SIGNAL
FROM DIS-22 PIO
TO C15-16 MEMORY CYCLE ENTIATE
ON POWER PANEL
MSB
LSB

2

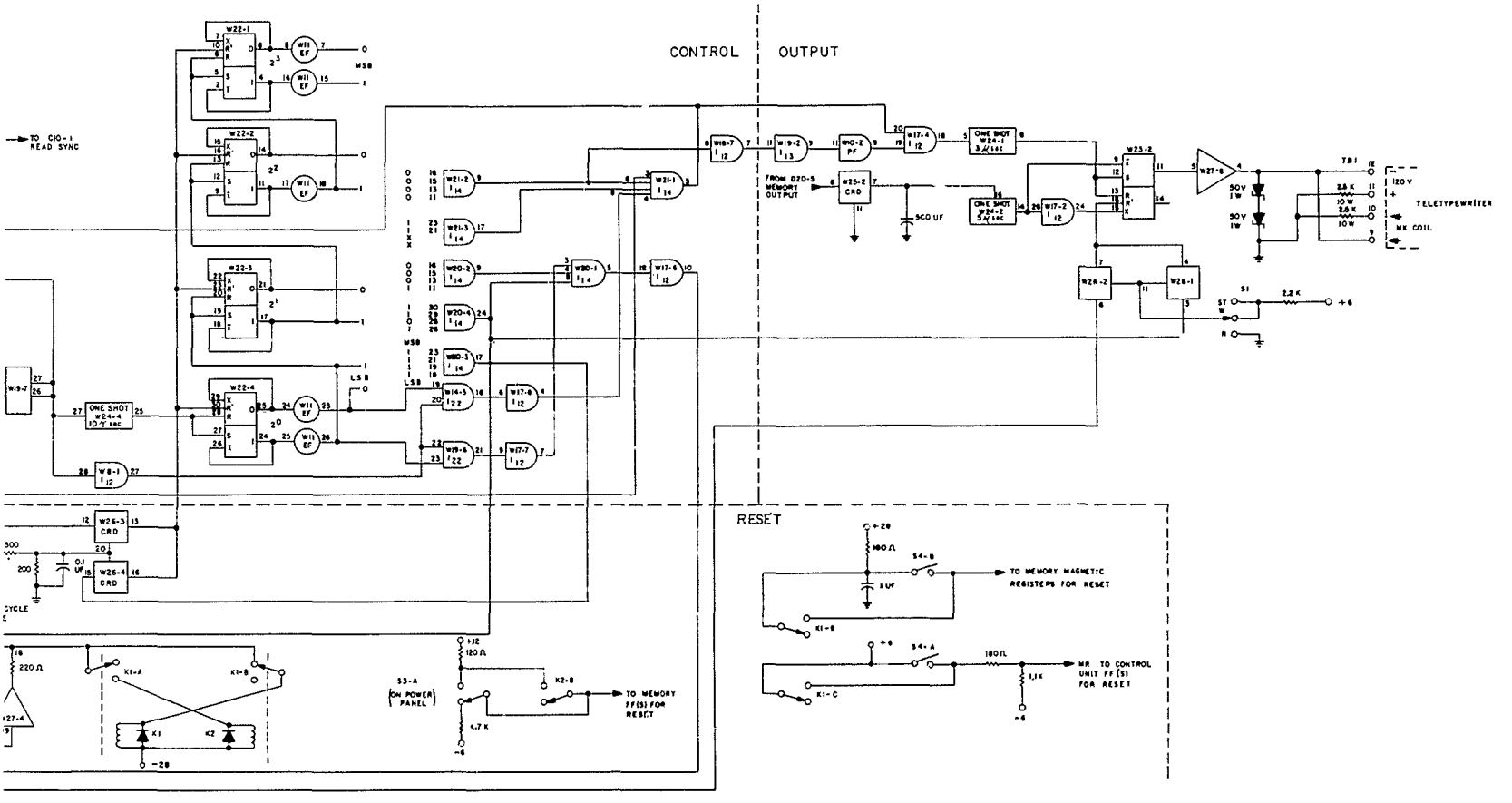


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Figure 3. DRISROTE Control Unit - Logic Diagram

The outputs of W-16-3 and W-18-2 are applied to gates W-7-2 and W-7-1 respectively where they are gated with the sampling pulse. If a mark is present during the occurrence of a sampling pulse, a logical "1" is stored in the memory. A logical "0" is stored for a space. The outputs of gates W-7-1 and W-7-2 drive the polarized return-to-zero circuit W-8. The output of this circuit goes directly to the DRISROTE memory. To inhibit information from the memory during the "Read" mode, an additional logic input is supplied to W-7-1 and W-7-2 by the control circuitry.

B. OUTPUT RECONSTITUTION

The information stored in DRISROTE is available serially from the memory output. The information is in the form of a positive, 6-volt, 0.25-microsecond pulse, imposed on a negative, 6-volt level for a logical "1", and no pulse for a logical "0". This is not compatible with the teletypewriter, and must therefore be suitably modified.

To accomplish this, the output pulses are lengthened to 5 microseconds by one shot W-24-2. This signal and its inversion are applied to flip-flop W-23-2 as control levels. Five "Read" pulses are generated by the control circuitry and applied to the flip-flop via one shot W-24-1. The flip-flop output will change in accordance with the information coming from the memory. Power amplification and level shifting is required to drive the teletypewriter. This is performed by driver W-27-8 and the 120-volt supply obtained from within the teletypewriter. The Zener diodes prevent the voltage induced by the teletypewriter coil from damaging the transistors.

To obtain proper operation, the flip-flop must be reset prior to each character generation. This is accomplished at the beginning of each "Read" cycle by switch S1 when it is manually turned to the "Read" mode. Following each character, the reset is performed by the "End of Character" signal generated by the control circuitry. This signal originates at gate W-20-4 and resets the flip-flop through gate W-26-1.

Flip-flop W-23-2 must also supply the start and stop pulses to the teletypewriter. The start pulse is generated by "setting" the flip-flop one bit ahead of the first information bit. The "set" signal is generated by gate W-21-2, shaped by circuits W-18-7, W-9-2, and W-10-2, gated by W-17-4, and delayed by one shot W-24-1.

At the end of the five information bits, the stop (reset) pulse is applied as described above as "End of Character."

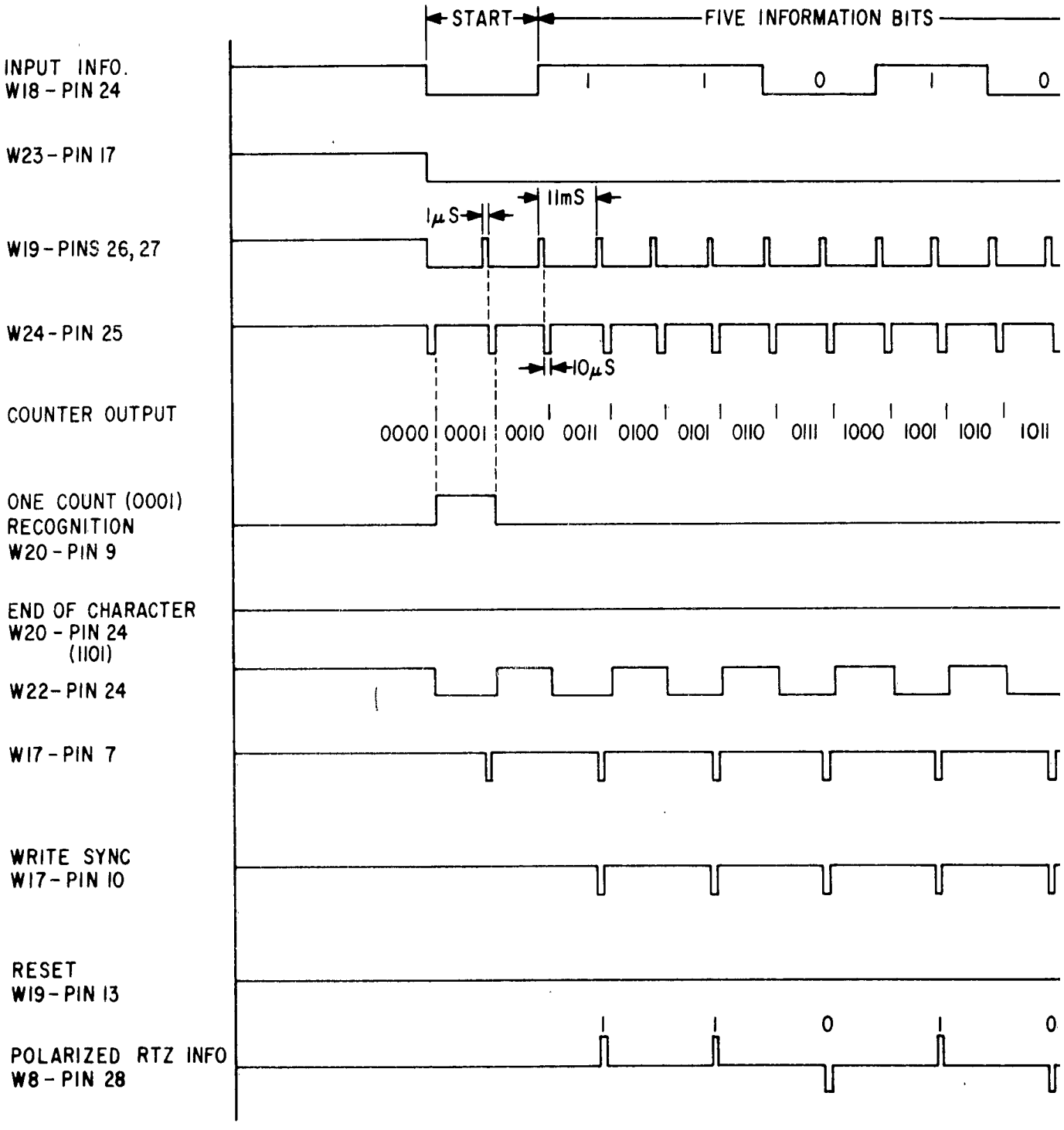
C. TIMING GENERATOR (Figures 4 and 5)

The basic clock, from which all timing and control signals are derived, consists of circuits W-16, W-23-4, W-25, W-19-7, and W-16-5. These circuits form a gated, free-running multivibrator. The clock is initiated whenever the "0" output of flip-flop W-23-3 is switched to the minus 6-volt level. This occurs at the beginning of each start pulse received from the teletypewriter during the "Write" mode. The start pulse is fed to the flip-flop via gate W-16-4. The clock is also initiated when the "Start" switch is closed during the "Read" mode. In this case, the pulse which triggers flip-flop W-23-3 is fed through gates W-6-8 and W-6-7.

The transition of the "0" side of flip-flop W-23-3 to -6 volts is gated through W-16 to flip-flop W-23-4. This complementing flip-flop is thereby triggered. One of the timing capacitors (S6) is charged and the Schmidt trigger W-19-7 is enabled. For a 60-WPM teletypewriter rate, the discharging capacitor will enable the Schmidt trigger for 11 milliseconds. As W-19-7 is switched off, the transistion is coupled back to flip-flop W-23-4 via gates W-16-5 and W-16. Flip-flop W-23-4 is complemented and the other timing capacitor is charged. The Schmidt trigger is then enabled for an additional 11 milliseconds. This process will continue until the "0" output of flip-flop W-23-3 is returned to ground. The waveform generated by W-19-7 is shown in Figure 4, as W-19-Pins 26, 27.

Flip-flops W-22-1,2,3, and 4 form a binary counter which counts the number of 11-millisecond intervals generated by the clock. Gates are used to recognize various counts for timing purposes. The gates are sampled by the inverted signal which drives the counter. To provide reliable recognition of counts, the input to the counter is delayed by one shot W-24-4. This prevents the state of the counter from changing during the sampling interval. Gate W-20-2 recognizes count 0001 which inhibits the first information sampling pulse during the "Write" mode. Count 1101 is recognized by gate W-20-4 and inhibits the seventh information sampling pulse. The second through to the sixth pulse are permitted to pass through gates W-20-1 and W-17-6 to sample the incoming information.

The sampling pulses are formed by inverting the clock output and passing it through gates W-19-6 and W-17-7. Flip-flop W-22-4 inhibits the even pulses from passing through W-19-6. The resulting signal is shown as W-17-pin 7 in Figure 4. The output of W-20-4 is also used via W-18-3 and W-19-4 to reset the counter and W-23-3, thereby stopping pulse generation. This reset function is allowed only during the write process by the control level input to W-19-4. The output of W-20-1 is inverted by W-17-6 and supplied to the input sampler W-7-1, 2 as write sync.


START
FIVE INFORMATION BITS
INPUT INFO.
W18 - PIN 24
1
1
0
1
0
W23 - PIN 17
1μS
11mS
W19 - PINS 26, 27
W24 - PIN 25
10μS
COUNTER OUTPUT
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011
ONE COUNT (0001)
RECOGNITION
W20 - PIN 9
END OF CHARACTER
W20 - PIN 24
(1101)
W22 - PIN 24
W17 - PIN 7
WRITE SYNC
W17 - PIN 10
RESET
W19 - PIN 13
1
1
0
1
0
POLARIZED RTZ INFO
W8 - PIN 28

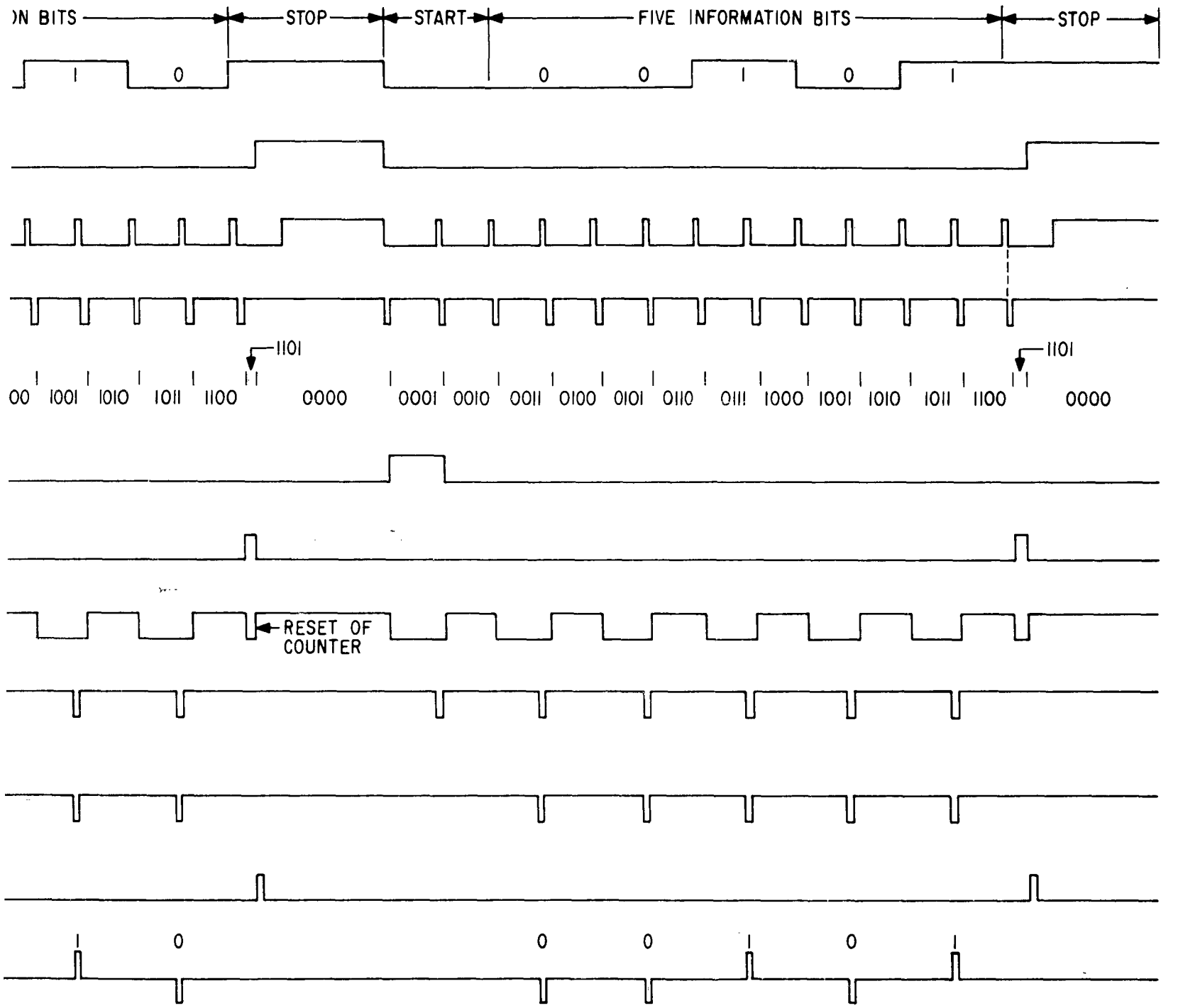
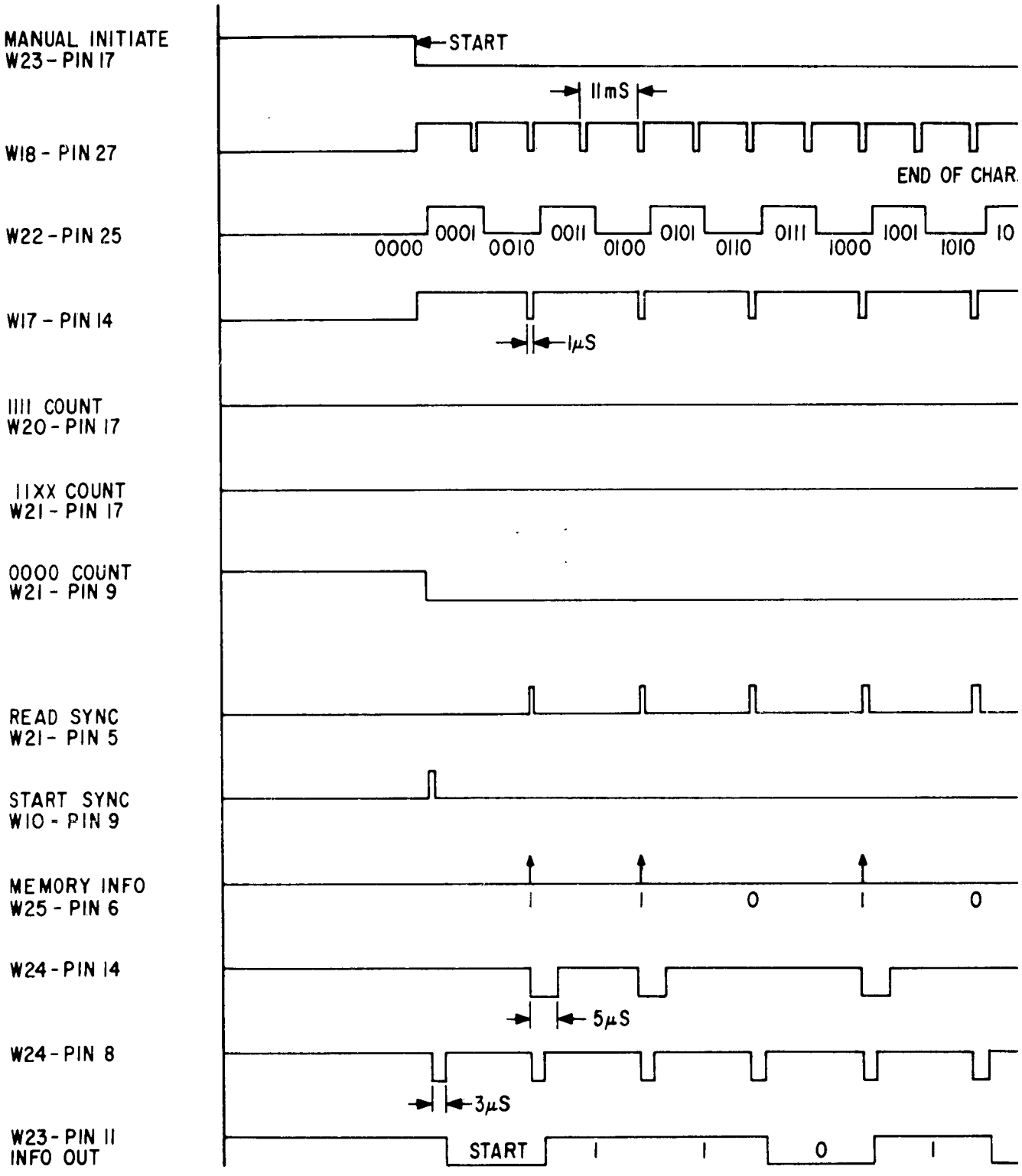


Figure 4. Teletype Adapter Waveforms - Teletypewriter Transmitting


MANUAL INITIATE
W23 - PIN 17
START
11mS
W18 - PIN 27
END OF CHAR.
W22 - PIN 25
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
W17 - PIN 14
1μS
IIII COUNT
W20 - PIN 17
11XX COUNT
W21 - PIN 17
0000 COUNT
W21 - PIN 9
READ SYNC
W21 - PIN 5
START SYNC
W10 - PIN 9
MEMORY INFO
W25 - PIN 6
1
1
0
1
0
W24 - PIN 14
5μS
W24 - PIN 8
3μS
W23 - PIN 11
INFO OUT
START
1
1
0
1

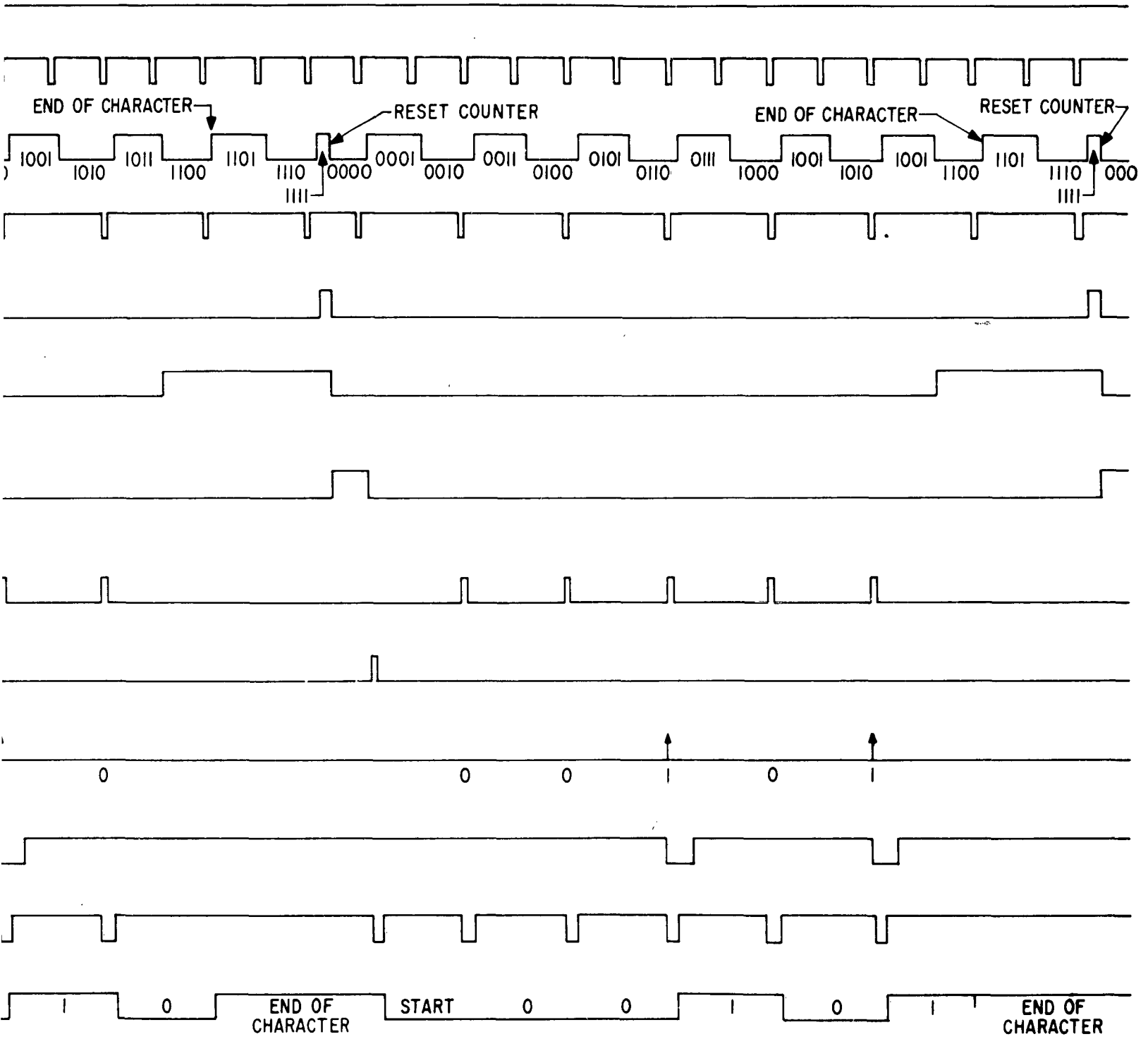


Figure 5. Teletype Adapter Waveforms - Teletypewriter Receiving

The output of W-14-5 is inverted by W-17-8 and supplied to W-21-1, where it is gated against the state of the counter as examined by W-21-2, 3 to suppress distribution of the starting transient and all pulses past the fifth even pulse. A control level is also supplied to W-21-1 to suppress all pulses during the "Write" mode. The output of W-21-1 is supplied to the reconstitution section as "Read Sync" and via the control section to DRISROTE as "Read Sync" (Figure 5). At the completion of 16 pulses (or 15 periods of the basic clock), gate W-20-3 supplies a signal to reset the counter only. This initiates generation of the next character without stopping the basic pulse generator. The output of W-20-4 is also supplied to the reconstitution section as an end of information signal for generation of the teletype stop signal.

When the DRISROTE memory is empty, a signal is generated which resets the counter and control flip-flops W-23-3 via W-19-3. This stops the system.

D. RESET SYSTEM

To insure that the memory and control unit always start correctly, all flip-flops and magnetic registers must be reset before starting an operation. When the Read-Write switch (Figure 3) is moved from standby to write, a positive level change is supplied to W-17-3 whose output triggers one shot W-24-3. This one shot activates a set of relay drivers (W-27-1, 2, 3, 4) which energize relays K_1 and K_2. This provides the required register and flip-flop reset signals. The two reset relays are connected to form an oscillator so that they are alternately energized as long as the drivers are ON.

When the read-write switch is moved from "write" to "read" the same function is performed by W-19-1, W-25-1, and W-24-3 etc., provided the memory has been filled. If the memory has not been filled, the outputs of flip-flop W-23-1 inhibit W-19-1. This allows W-16-1 to pass a signal to initiate a transfer of the DRISROTE input register content to the memory and results in clearing the input register. At the completion of this transfer, a pulse (P-10) is returned to the adapter and via W-6-1 to the reset system. At the time the read-write switch is moved, one shot W-29-1 produces a 15-microsecond gate pulse to allow only the first P-10 pulse to energize W-24-3 and the reset sequence. The contacts of the reset relays parallel the function of the manual reset switches and provide the reset for the timing generator.

E. CONTROL

A step-by-step description of the "write" and "read" cycle are presented here to explain the operation of the control logic. The logic block numbers refer to Figure 3.

Write Cycle

The control level from S1 moves from -6 volts to 0 when switching from "standby" to "write". This level change is used to initiate the reset cycle and is inverted by W-18-6 to partially enable W-5-5. When the first teletype key is depressed, the signal it generates moves from 0 to -6 volts which is applied via double inversion of W-16-3 and W-18-2 to W-7-1, W-5-5 and W-16-4. W-5-5 is enabled to set W-1-1 whose output now unblocks the sampler W-7-1, 2 and the output is summed with the teletype signal in W-16-4 to set W-23-3, the timing generator control. Following this, the timing generator provides five sampling pulses to the sampler W-7-1, 2 as described in paragraph C, and then resets W-23-3 which stops the timing generator. This sequence of pulses is shown in Figure 4.

When the next teletype key is depressed, the same signal routing is provided to the sampler, and the double inverted signal is inverted by W-16-4 to set W-23-3 for starting the timing generator. Pulse generation and reset are as before. Reset of the timing generator via W-19-4 is permitted by the application of the inverted control signal to one of its inputs. This process continues until there is space for only twelve more characters in the memory. At this time, C-14-24 in the memory supplies a signal to W-27-5 to operate a warning lamp. When the memory is filled, flip-flop W-1-2 is set to extinguish the warning lamp. The output of W-1-2 is also utilized to set W-29-4 whose output enables W-27-7 to activate the "memory full" lamp. The "memory full" pulse also resets W-1-1 to disable the sampler and inhibit triggering of the timing generator via W-16-4. In addition, the "memory full" signal sets W-23-1 in the reset control to disable the memory cycling function during reset.

Read Cycle

Movement of S1 to the "Read" position supplies the level change of 0 to -6 volts to W-18-6, the reset circuit, and W-21-1 to enable distribution of the "Read Sync". The reset system initiates information transfers where required and returns the memory to the starting position ready for initiation of the readout function.

Actuation of the start button energizes the logic chain W-1-4, W-6-7, W-6-8, W-9-4, and W-10-4, to produce a positive pulse at S1-Y. This pulse sets W-2-1 whose output supplies an enable signal to the memory. This permits information transfer to the output register and supplies one of the control levels to W-7-3. The pulse at S-1-Y is also routed via W-18-4 and W-18-5 to the memory to initiate transfer of the first 64-bit information block to the output

register. Upon completion of this transfer, a memory-generated signal sets W-1-3 via W-6-1 and W-6-2. The output of W-1-3 supplies the second control level to W-7-3, whose output sets W-2-2; this enables W-6-3 to pass "Read Sync" pulses to the memory.

The output of W-7-3 also sets W-23-3 in the timing generator control to start generation of the "Read Sync" and associated pulses. Operation of the timing generator proceeds as described in paragraph C, furnishing the appropriate sync and control pulses to reconstitute the original message. This sequence of pulses is shown in Figure 5.

When the memory is empty, it supplies a signal to reset W-1-3, W-2-1, W-2-2, and W-23-1. W-2-1 now inhibits information transfer to the output register. W-2-2 blocks W-6-3, preventing distribution of "Read Sync" pulses to the memory. W-2-2 also sets W-29-3 whose output operates the "memory empty" indicator via W-27-6, and via W-19-3 resets the counter W-22 and timing generator control W-23-3. This stops the readout process. If it is desired to stop the readout before completion of 3072 characters, the "stop" button may be manually depressed which resets W-23-3 and W-23-2, ending readout and teletype operation.

F. NEW CIRCUITS

One Shot

This circuit is a modified DR-3 and is shown in Figure 6. A negative transition at the input turns Q_1 ON and Q_2 OFF via "C" for a period determined by "C" and R1. The output is a negative pulse. When an external CRD gate is used to supply an input at the base of Q_2, the circuit may be triggered with positive pulses.

Lamp Driver

This circuit is basically a DR-1-B without collector resistors. It is shown schematically in Figure 7. The transistors are high voltage units. Four of the circuits on the board (Figure 12) have 220-ohm resistors in their output for current-limiting, and are used to drive the reset relays.

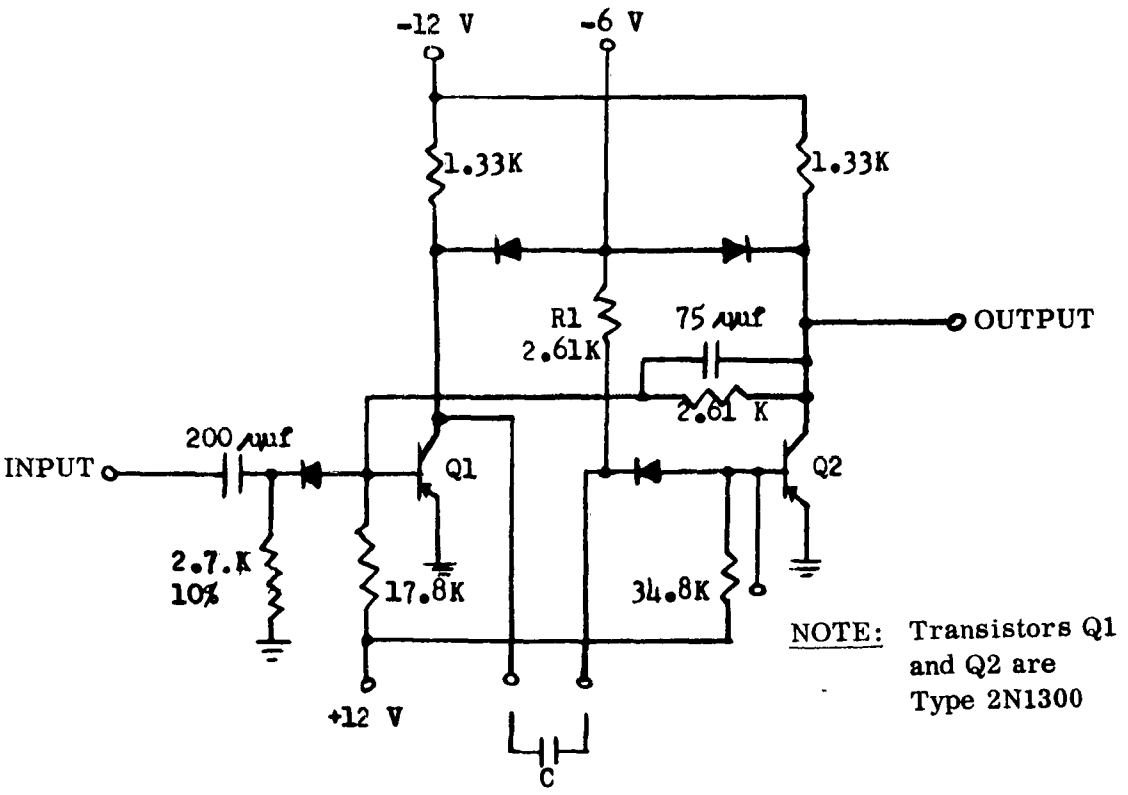


Figure 6. One Shot Circuit - Schematic Diagram

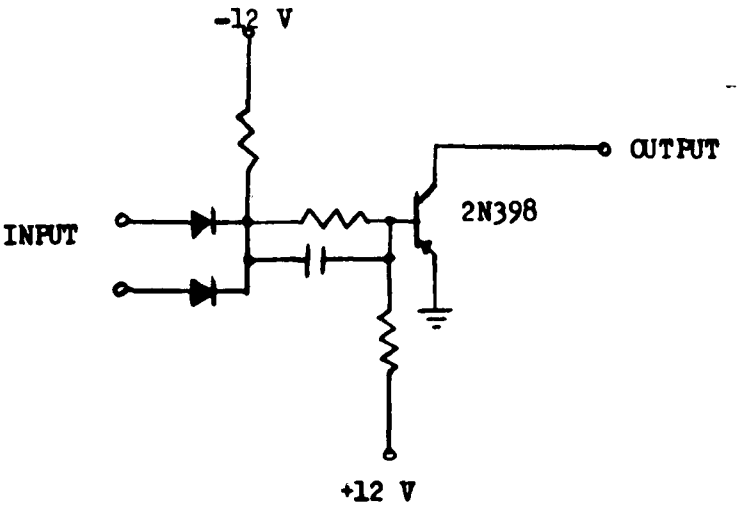


Figure 7. Lamp Driver Circuit - Schematic Diagram

Delay and Schmidt Trigger

This circuit is shown in Figure 8. Components of this circuit are mounted as follows: A, B, and C are on the CRD gate board, the capacitors are located on the speed switch, and the remainder on a modified DR1-B board, taking the place of the seventh and eighth circuit.

When either of the two inputs moves from -6 volts to ground, the resulting signal is coupled by "C" to the base of Q_1 which is turned off; this in turn turns on transistor Q_2. The period of time in this state is determined by "C" and R1. As the voltage on the Q_1 base returns to the voltage of the Q_2 base, Q_1 is turned on, with current switching from Q_2 enhancing the turn-on. Thus, for a positive level shift at either input, the output is a negative-going pulse for a time determined by "C" and R1. Because the two inputs may be alternately used (i.e. when fed by a flip-flop), this circuit will produce long negative pulses separated by fractions of microseconds without any recovery problems.

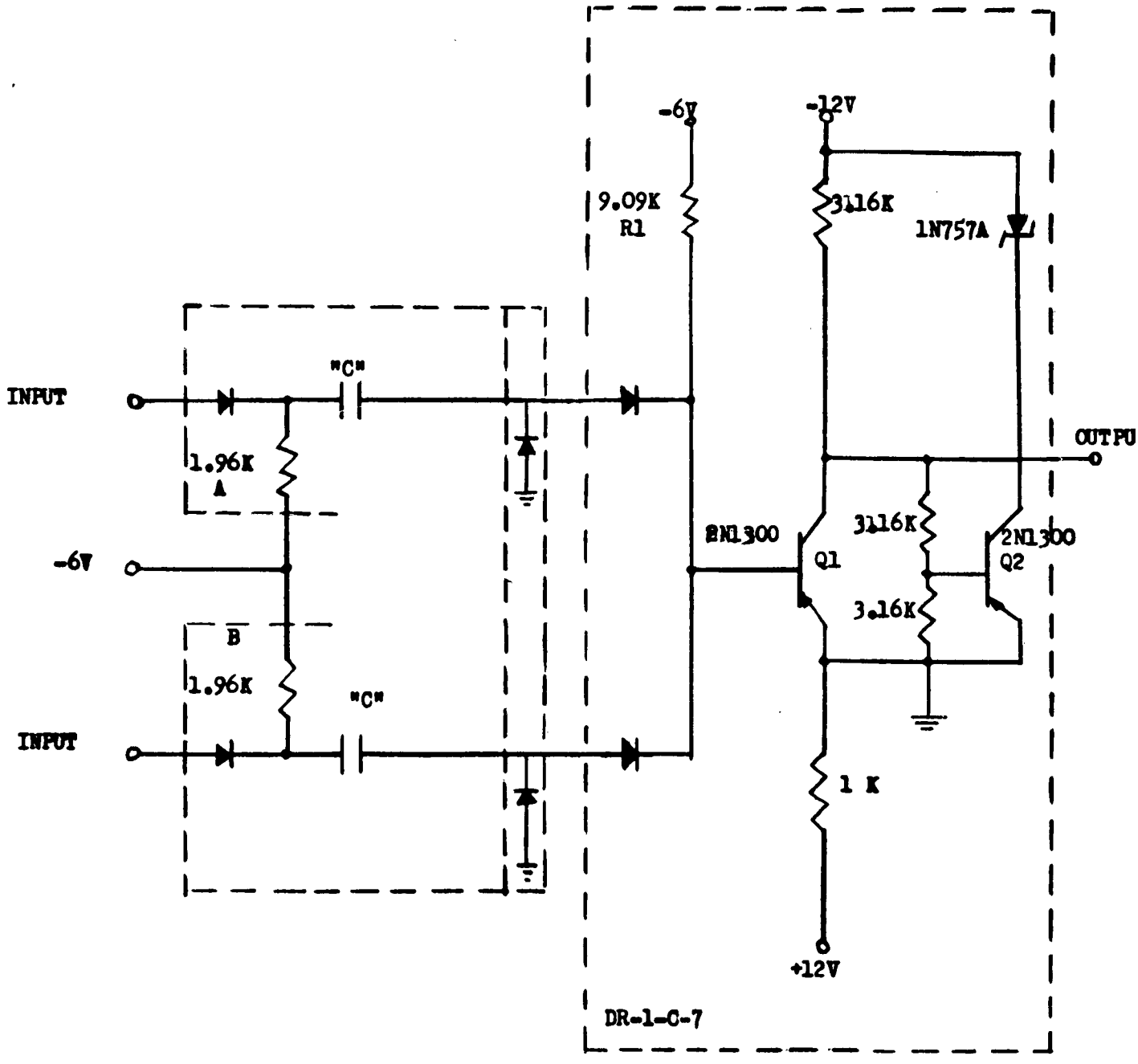


Figure 8. Delay and Schmidt Trigger - Schematic Diagram

SECTION V

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

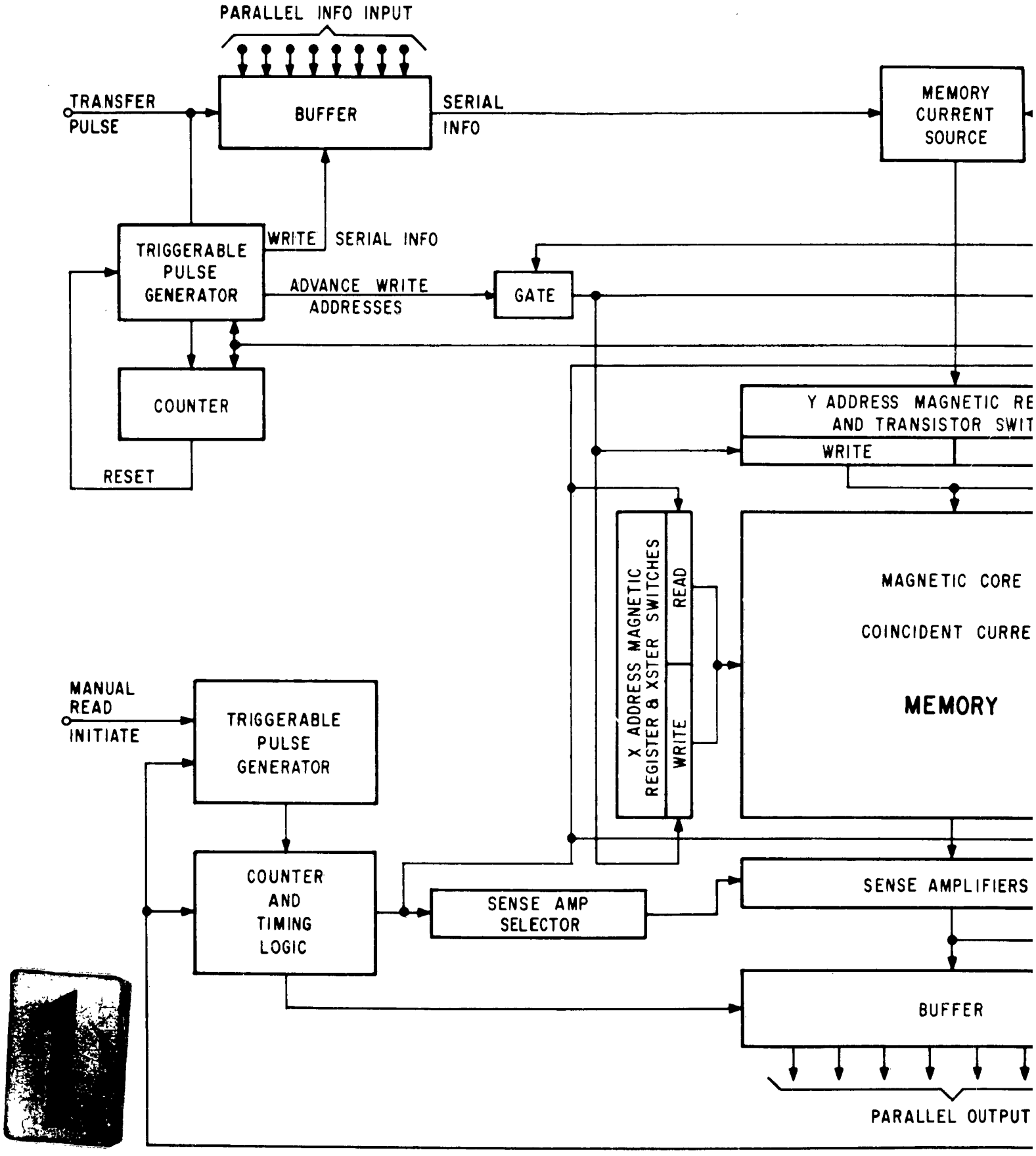
The state of the electronic art is constantly providing new components and techniques. Many have become available since the inception of the DRISROTE program. Some of these would contribute to a better fail-safe design to an equipment such as DRISROTE. This factor and the large number of operating hours accumulated has contributed in large part to the difficulty in using DRISROTE for the storage of teletypewriter-generated data.

Although the present system performs satisfactorily, it must be recognized that optimum performance can only be obtained by designing a system for the intended application. Figure 9 shows the system proposed for the teletype time compression memory. A maximum degree of flexibility has been incorporated. Information can be accepted in either serial or parallel form. Since both five and eight-bit parallel word teletypewriters are in common use, provision has also been made to accommodate this variable. The same flexibility has been incorporated into the read-out operation. The specific mode desired is determined by the operator, and the Mode Selector shown in Figure 1 can be set to the appropriate position.

The information input and output rates are independently variable and are also controlled by the Mode Selector. The information rates can be varied in discreet steps to accommodate the lowest teletype speed and the highest transmission bit rate. This is approximately 750 KC.

The capacity of the proposed memory is approximately 10,000 bits. This is sufficient to store a full page of information. The capacity can be easily increased without changing the basic concepts of the system.

The memory system proposed is quite unique in that is uses only a single current source for the entire memory. Selection of a desired location in the memory is made by advancing the three magentic registers simultaneously. Each register is associated with one of the planes in the three-dimensional array. As the three registers are advanced each enables a transistor switch. The current from the single source is then steered through the memory on a unique


PARALLEL INFO INPUT
TRANSFER PULSE
BUFFER
SERIAL INFO
MEMORY CURRENT SOURCE
TRIGGERABLE PULSE GENERATOR
WRITE
SERIAL INFO
ADVANCE WRITE ADDRESSES
GATE
COUNTER
RESET
Y ADDRESS MAGNETIC RE
AND TRANSISTOR SWIT
WRITE
X ADDRESS MAGNETIC REGISTER & XSTER SWITCHES
READ
WRITE
MAGNETIC CORE
COINCIDENT CURRE
MEMORY
MANUAL READ INITIATE
TRIGGERABLE PULSE GENERATOR
COUNTER AND TIMING LOGIC
SENSE AMP SELECTOR
SENSE AMPLIFIERS
BUFFER
PARALLEL OUTPUT

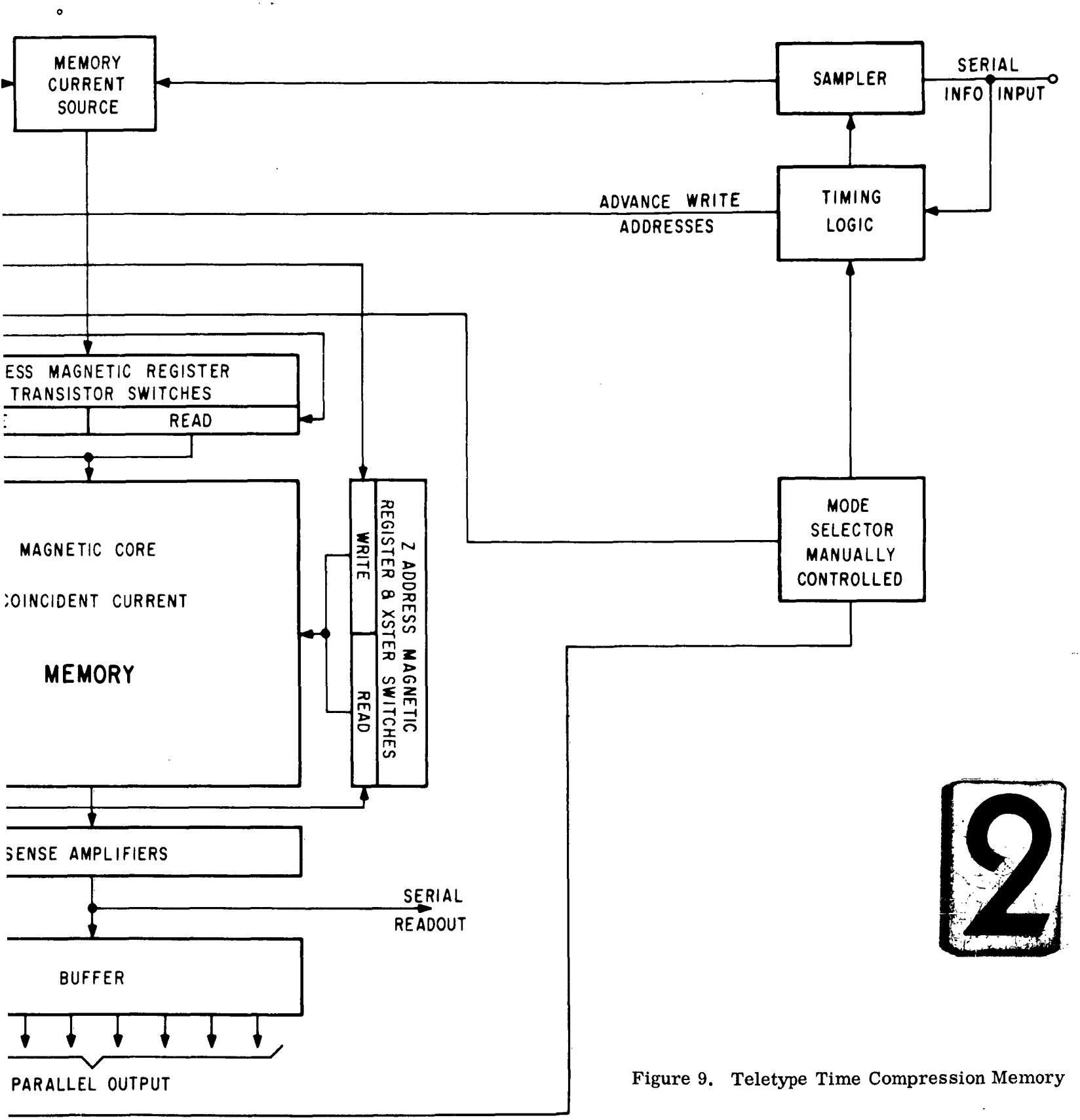


Figure 9. Teletype Time Compression Memory

path which selects a single location. The registers are so arranged that the entire memory is selected bit-by-bit with each advance of the registers. Read-out is accomplished in the same manner.

This approach eliminates the many drivers normally associated with memories, as well as the need for a diode steering matrix. The net result is an increase in reliability and a decrease in the number of components.

All logic and timing is generated with transistor switching circuits.

APPENDIX

OPERATION AND MAINTENANCE INSTRUCTIONS

Several precautions must be observed when placing the unit in operation. These are listed below in their order of importance.

1. Ascertain that the two plugs on the DRISROTE are in their proper place and are securely seated.

2. Connect a ground wire from the frame of the DRISROTE to the power supply ground terminals on the adapter frame. Wire must be at least #16.

3. Make certain all power supplies are ON and at their proper voltage before moving any of the power control panel switches to the ON position.

4. Place the "Read-Write" switch to the OFF position when turning on power.

5. To apply power to the unit, the following switching sequence on the power control panel must be followed:

   S1, S2, S3, Reset, S3, Reset, S4, S5, S6, S7, S8, S9, Reset S3, Reset.

6. Place S5 on the adapter in the teletype position.

7. Turn on the teletype machine and place its control switch in Position #1.

8. Turn the "Read-Write" switch on the adapter control panel to the "Write" position.

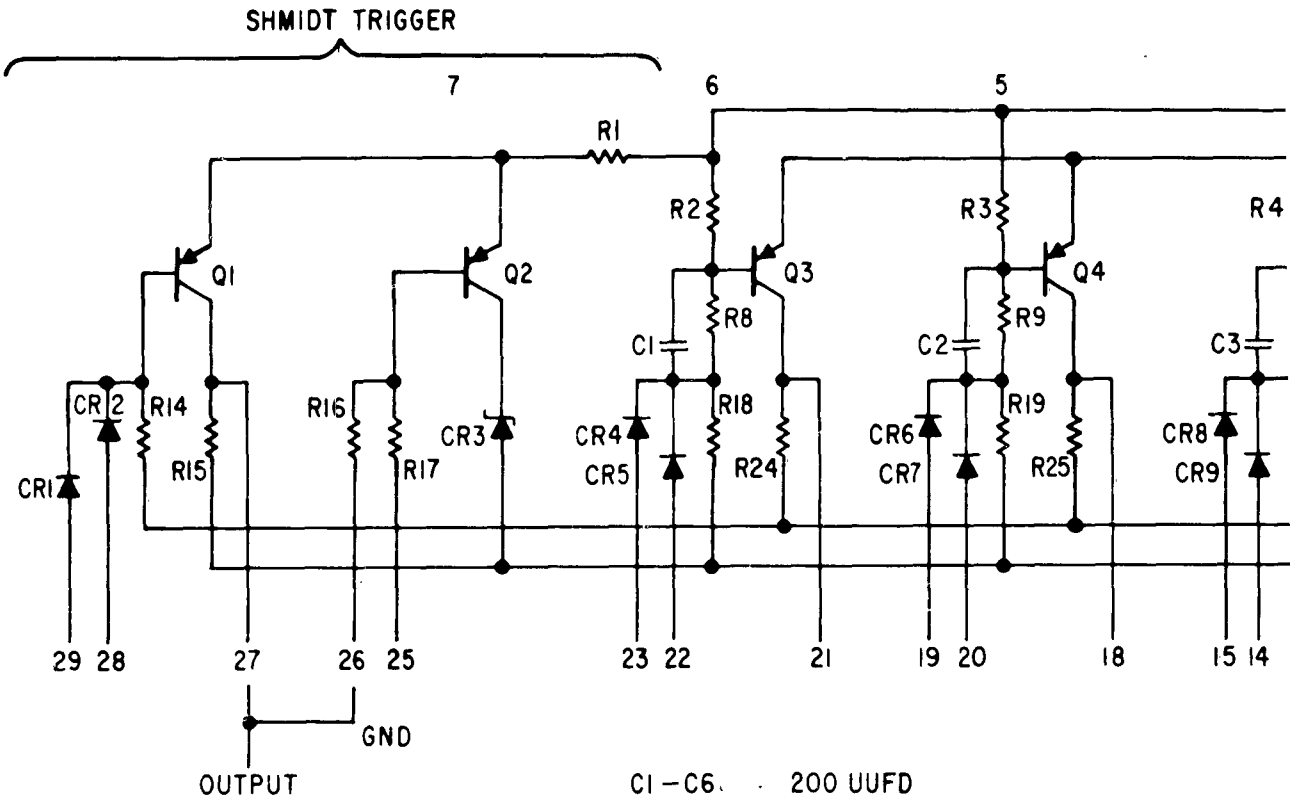
The system is now ready to type information into the memory.

After the message is stored, it is only necessary to switch the "Read-Write" switch to the "Read" position and to depress the "Start" switch.

If a failure should occur, the reader is referred to Section IV-E and Figure 3 for signal tracing within the adapter/control unit. If the failure occurs within the DRISROTE, the reader is referred to "Preliminary Instructions for the Operation and Maintenance of DRISROTE Memory Unit".*

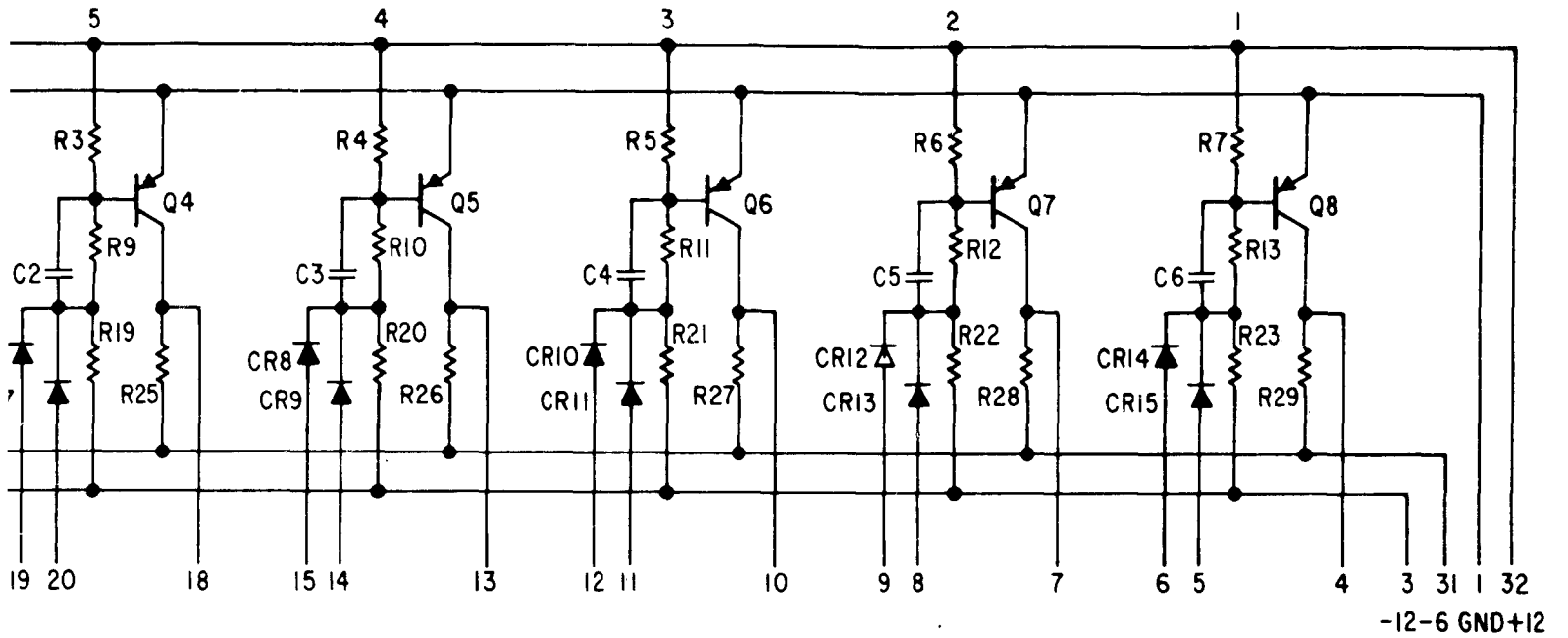
As an aid in troubleshooting, the board schematics which are different from the standard boards are included here (Figures 10 through 14). All of the indicated external connections and voltages must be applied for proper operation of the circuits.

*This report was submitted to the Air Force as partial fulfillment of the requirements on Contract No. AF 33(616)6230, DRISROTE.



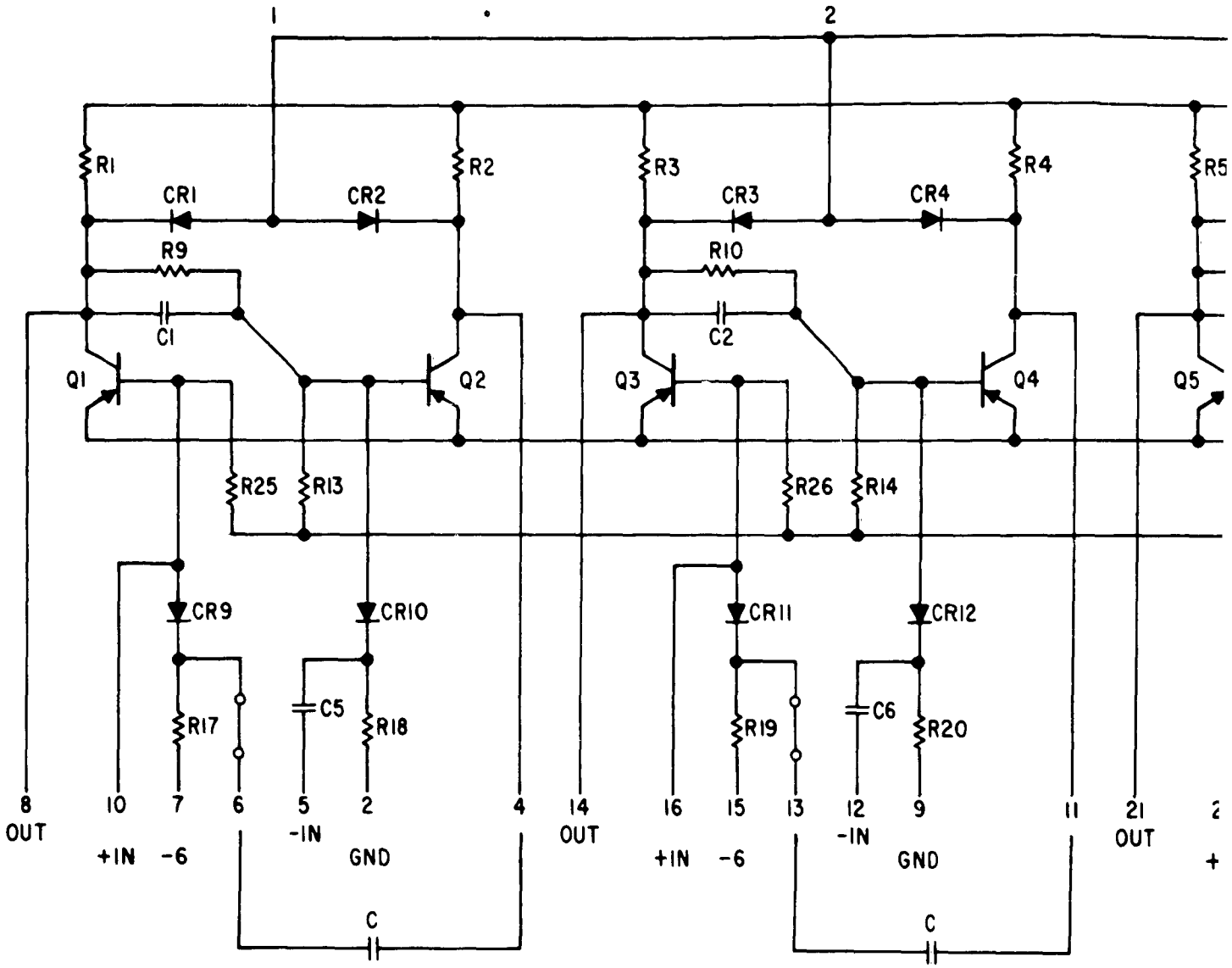
C1 – C6	200 UUFD
CR1, 2, 4 – CR15	IN695
CR3	IN757A
Q1 – Q8	2N1300
R1	1K 1/8W 1%
R2 – R7	6.81K 1/8W 1%
R8 – R13	750Ω 1/8W 1%
R14	9.09K 1/8W 1%
R15, R16	3.16K 1/8W 1%
R17	316Ω 1/8W 1%
R18 – R23	2.15K 1/8W 1%
R24 – R29	1.47K 1/8W 1%

DRI-C



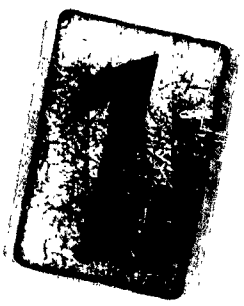
% 1%
1%
1%
1%
1%
1%
1%

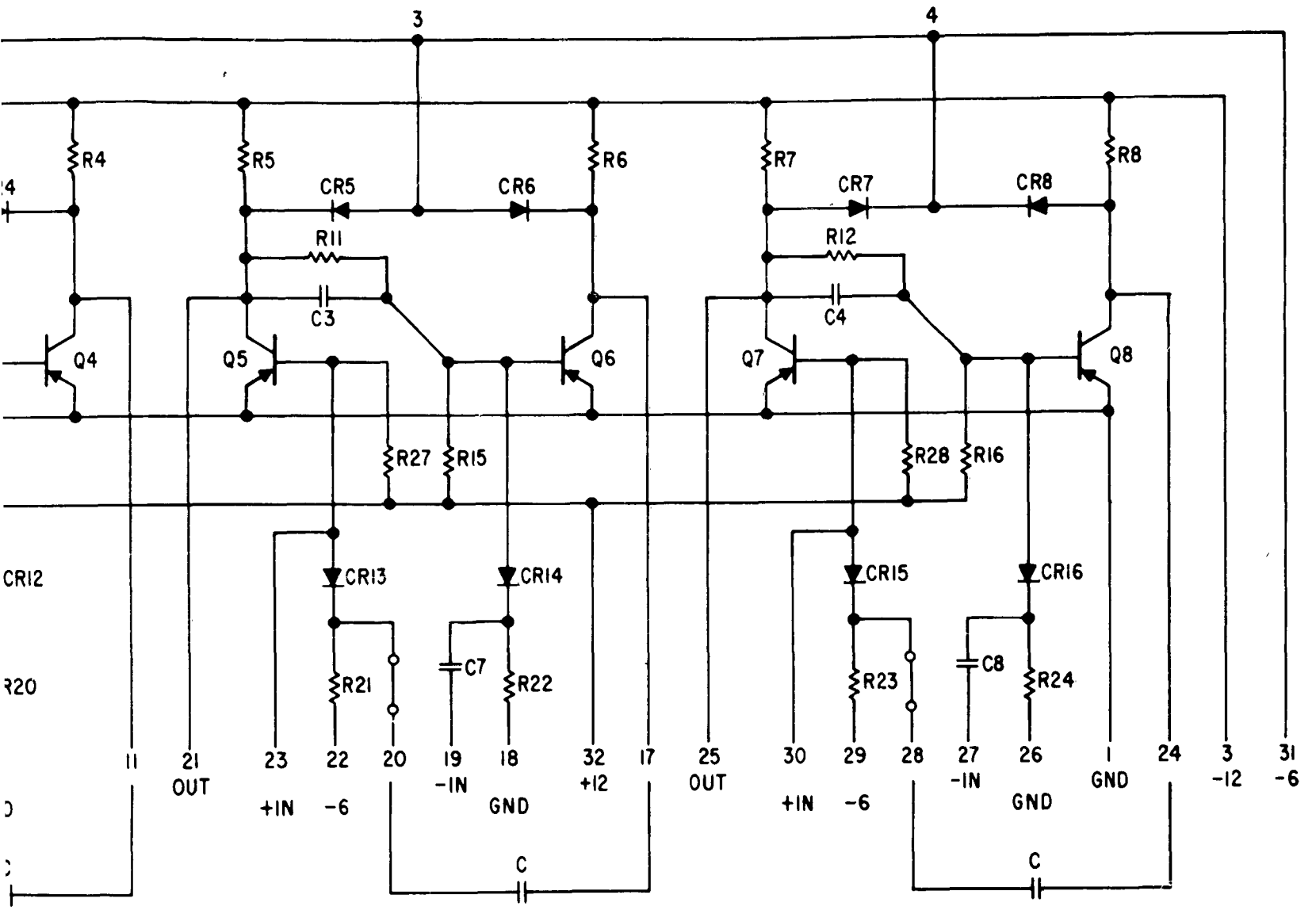
Figure 10. Schmidt Trigger and Power Inverters - Schematic



C1-C4	75UUFD
C5-C8	200UUFD
CR1-CR16	IN695
Q1-Q8	2N1300
R1-R8	1330Ω 1/8W 1%
R9-R12	2610Ω 1/8W 1%
R13-R16	17.8KΩ 1/8W 1%
R17, 19, 21, 23	2610Ω 1/8W 1%
R18, 20, 22, 24	2.7K 1/4W 1%
R25-28	34.8K 1/8W 1%

NOTE: C IS SELECTED FOR THE
C = 1000 UU t = 2
C = 280 UFD t = C





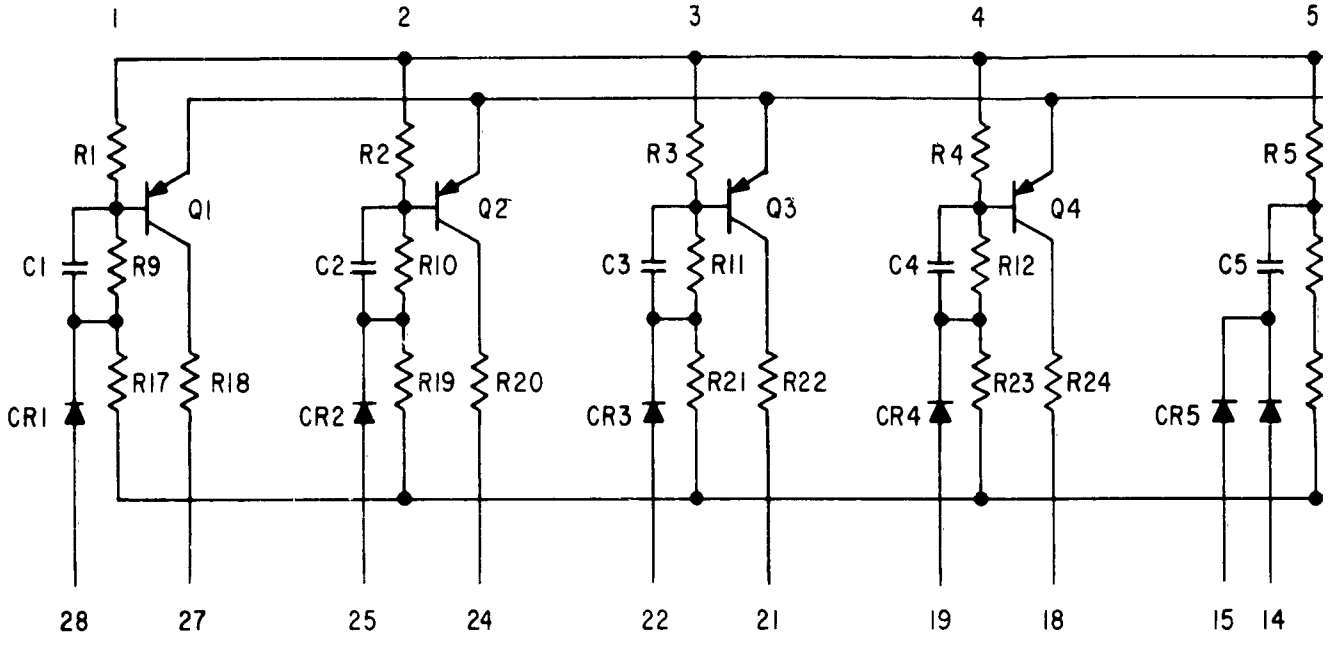
C IS SELECTED FOR THE REQUIRED DELAY

C = 1000 UU t = 2 U. SEC

C = 280 UFD t = 0.5 SEC

2

Figure 11. One Shot - Schematics



C1–C8	200 UUFD
CR1–CR9	IN695
Q1–Q8	2N398
R1–R8	6.81K 1/8 1%
R9–R16	750Ω 1/8W 1%
R17,19,21,23,25,26,27,28	2.15K 1/8W 1%
R18,20,22,24	220Ω 1/2W 10%

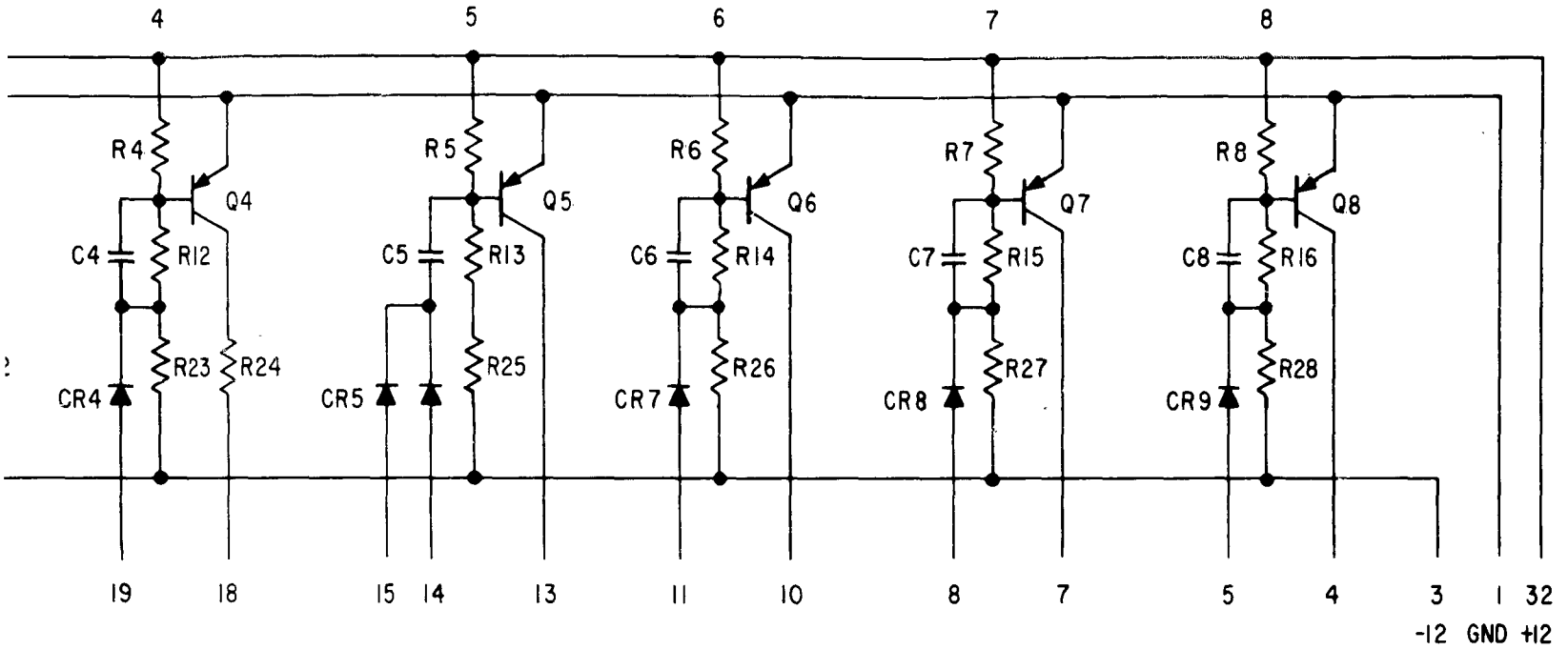
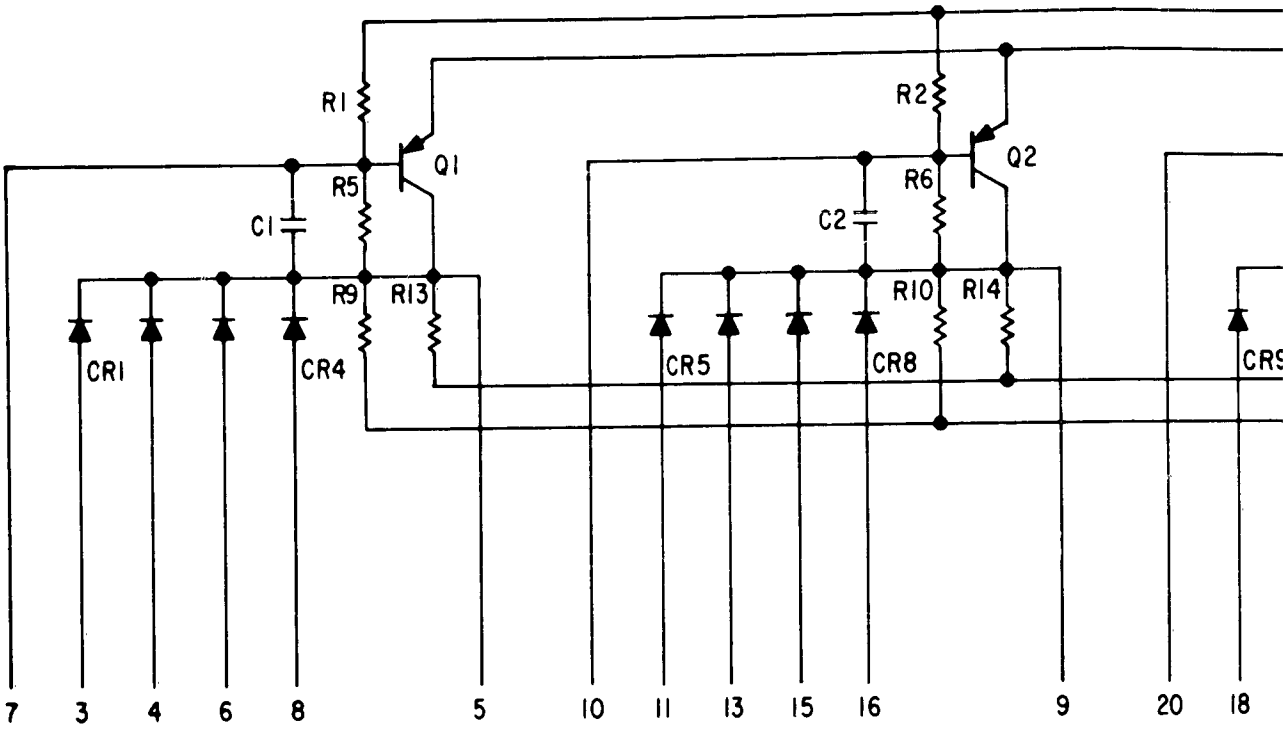


Figure 12. Lamp and Relay Drivers



C1 – C4	100 UUFD	
CR1– CR16	IN695	
Q1 – Q4	2N1300	
R1 – R4	9090Ω	1/8 W 1%
R5 – R8	1210Ω	1/8 W 1%
R9 – R12	3480Ω	1/8 W 1%
R13– R16	1960Ω	1/8 W 1%

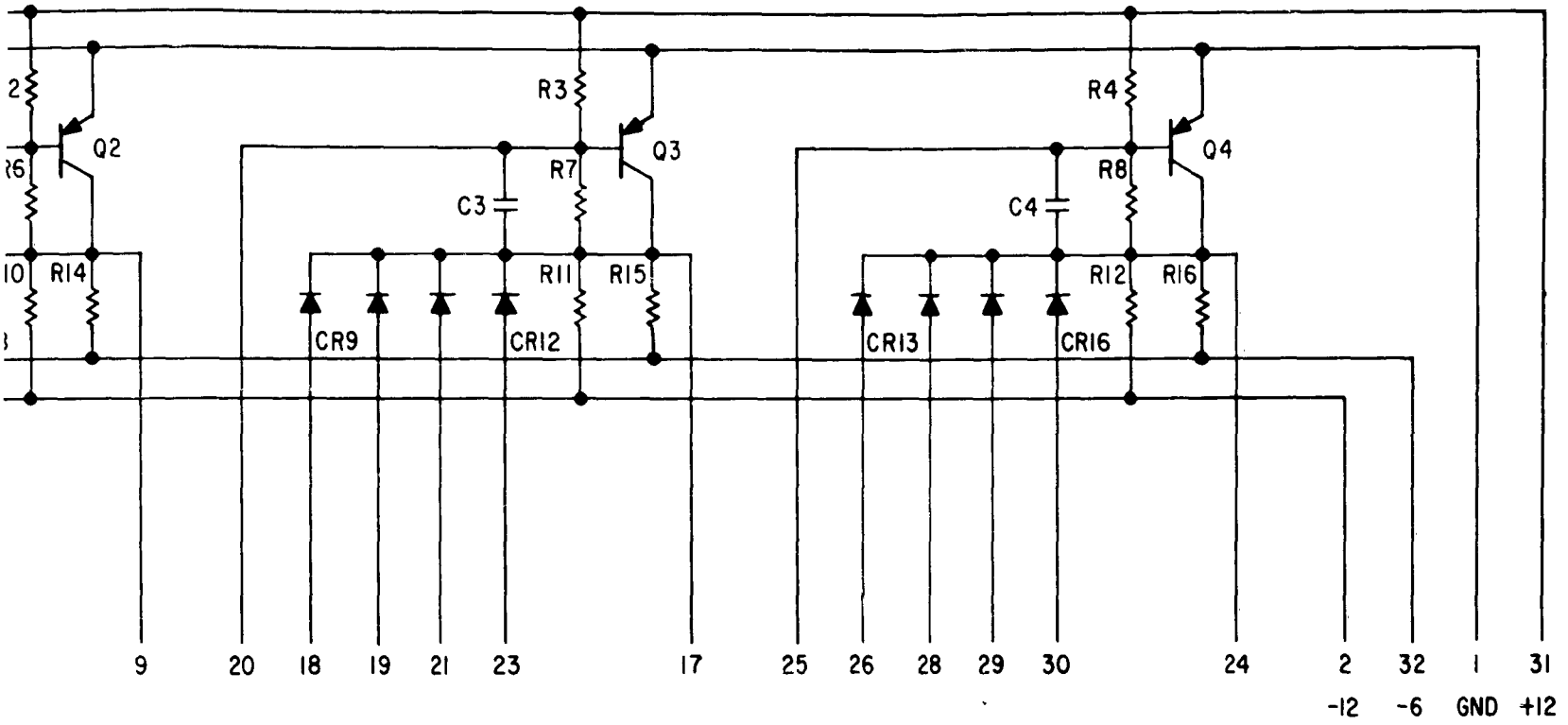
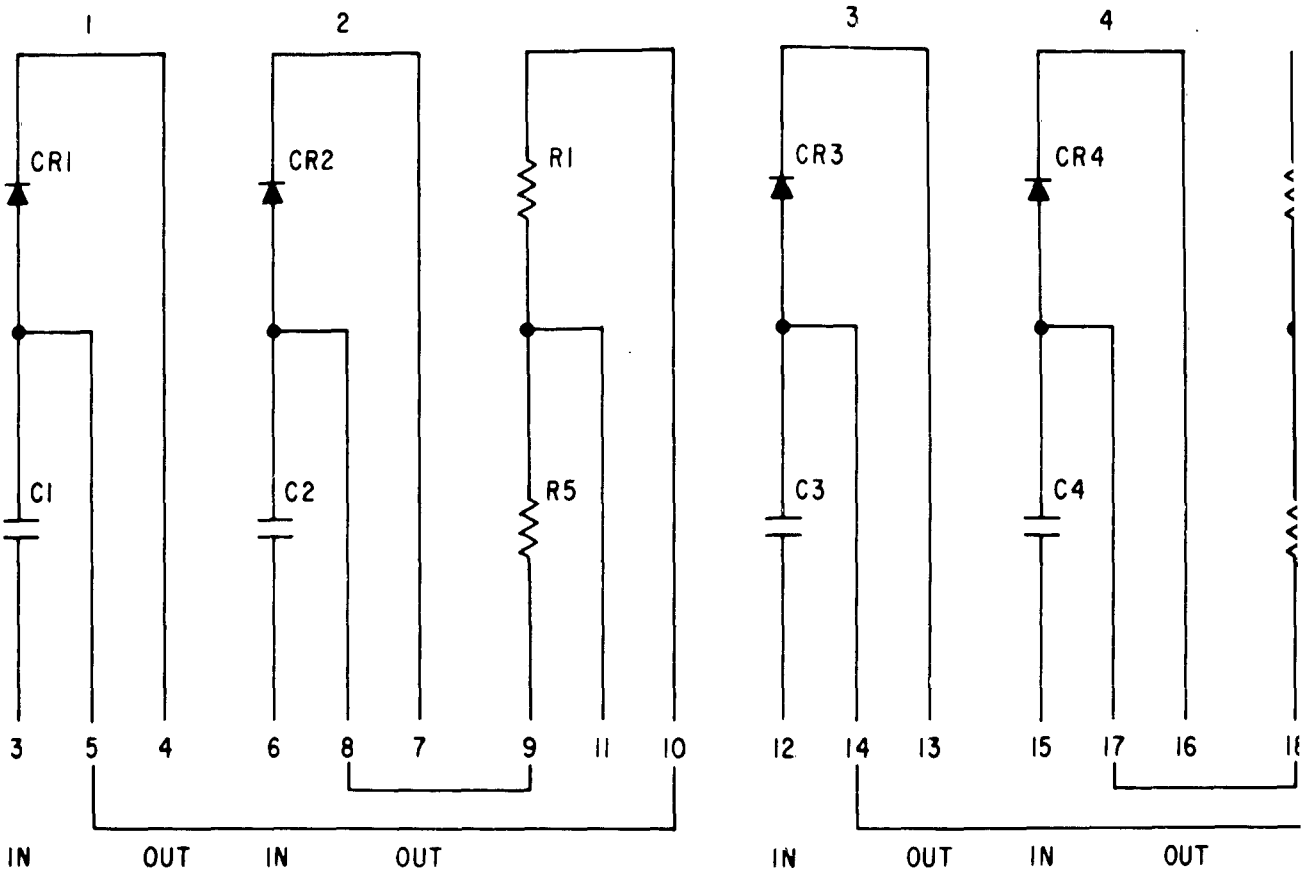
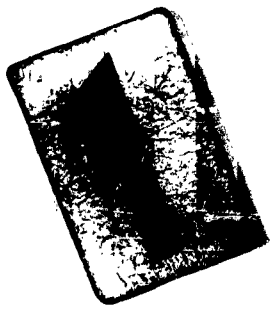


Figure 13. Four-Input Inverters



C1 – C4	1000 UUFD	
CR1-CR8	IN695	
R1,2,5,6	2.7K	1/4W 5%
R3,4	1.96K	1/8W 1%



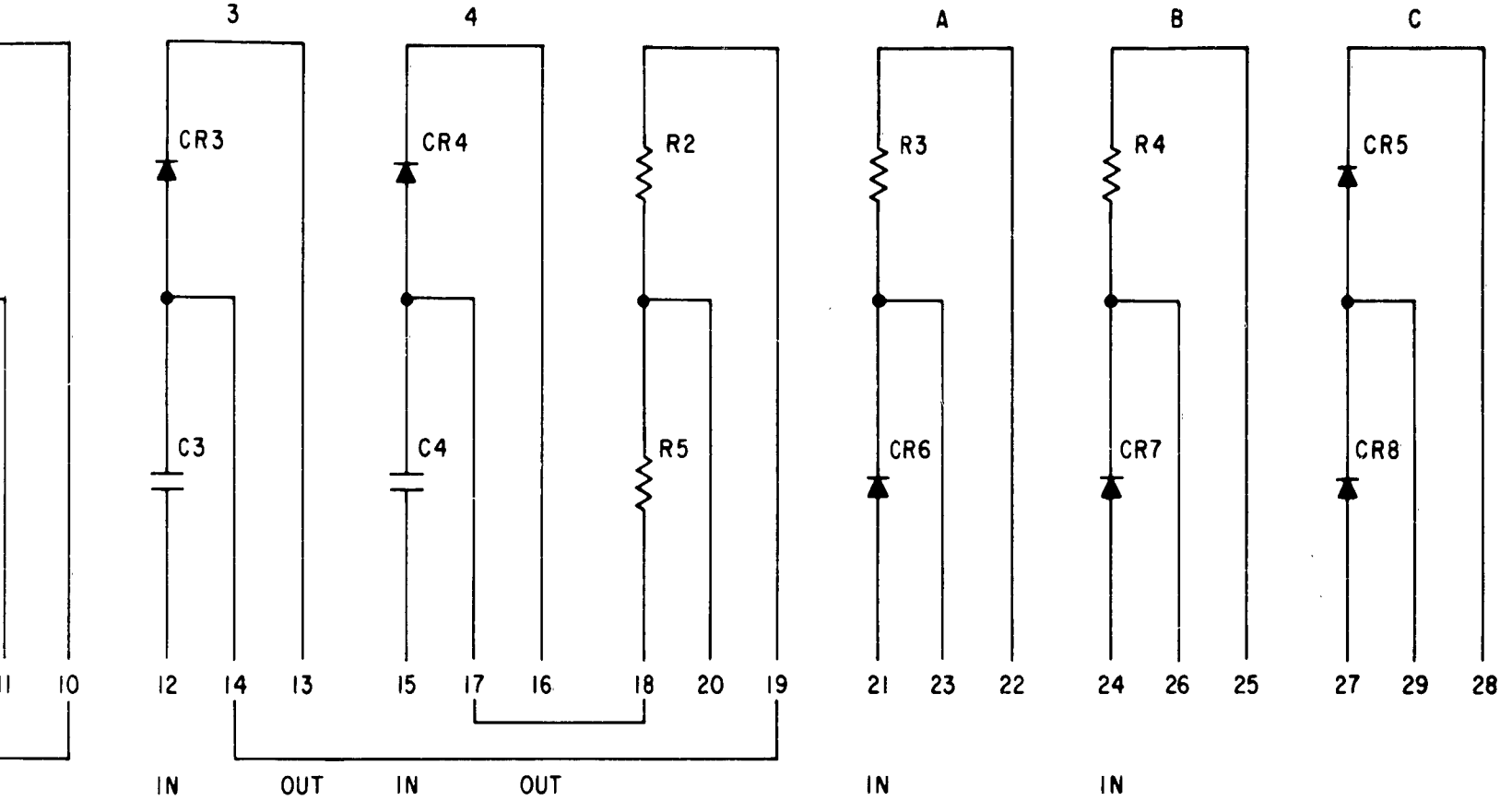


Figure 14. CRD and OR Gates

Electromagnetic Warfare and Communications Laboratory Aeronautical Systems Division, Dir/ Avionics, Wright-Patterson AFB, Ohio. Rpt. Nr. ASD-TDR-62-1058, A TELETYPEWRITER ADAPTER UNIT FOR THE DRISROTE APERTURED PLATE MEMORY. December 1962. 30 p. incl. illus, & tables. (Project 4335; Task 433517) (Contract AF33(657)-7905 Unclassified Report)

This task was initiated to demonstrate the use of the DRISROTE equipment AF33(616)-6230 as a storage device for teletypewriter information. The particular teletypewriter used is a Kleinschmidt Model 120 which utilizes serial 7.42 unit

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II Contract AF33(657)-7905

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Electromagnetic Warfare and Communications Laboratory Aeronautical Systems Division, Dir/ Avionics, Wright-Patterson AFB, Ohio. Rpt. Nr. ASD-TDR-62-1058, A TELETYPEWRITER ADAPTER UNIT FOR THE DRISROTE APERTURED PLATE MEMORY. December 1962. 30 p. incl. illus, & tables. (Project 4335; Task 433517) (Contract AF33(657)-7905 Unclassified Report)

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II Contract AF33(657)-7905

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Baudot Code. The DRISROTE equipment is an apertured plate memory capable of storing 15,360 bits of information with input and output rates up to one megacycle. To achieve the objective, an adapter was designed and constructed, and modifications were made to the teletypewriter and DRISROTE. Teletypewriter-generated messages were stored in DRISROTE, reconstituted, read out of DRISROTE, and printed by the teletypewriter with good fidelity.

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